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ADL-P MB Schematic Document

LA-L655P

Rev: 1.0

2021.04.15

ZZZ
PCB 3LP LA-L655P REV1 M/B TRIPOD A31 !
DAA000SD011
SIF_MLK_PCB@

ZZZ
PCB 3LP LA-L652P REV1 M/B TRIPOD A31 !
DAA000RC011
AXIOM_PCB@

@ : Un-pop Component
@EMI@/@ESD@/@RF@ : EMI, ESD, RF Un-POP Component
EMI@/ESD@/RF@ : EMI, ESD, RF Component
JUMP@/JP@/PJP@ : JUMP
5VFAN@/12VFAN@ : JUMP for FAN power
XDP@ : XDP Component
CONN@ : Connector Component
SW@ : Debug PWR But t on
CNV@/@CNV@ : CNVi Support
G3@ : EC G3 Flash Sharing
N18P@/GN20P@ : GPU Support
GN20P0@/GN20P1@ : P0 or P1 SKU
VS8GR3@/VM8GR3@/VH8GR1@ : VRAM SKU
VS@/VM@/VH@ : VRAM Support
BBY@ : BBY Support

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Block Diagram

eDP CONN P.38
eDP MUX PI3WVR13612ZLEX P.39
eDP 1.4b
P.6~P.118
DDR5 Channel A 4800 MT/S
DDR5 So-DIMM *2 P.23~P.24

GDDR6 VRAM *4 P.40
HDMI 2.1
HDMI CONN P.40
HDMI 2.1
VBIOS ROM 2M P.30
HDMI 2.1
V
N idia GPU
GN20P 80W
GN20P-R(UI) P.26~P.37
PEG Gen5 *8

DP2 / USB3.2 / AUX
USB Type-C CONN P.45
VBUS / CC
Nuvoton PD PTPS65992SA0CRSMR P.44
CC
USB 2.0
USB 2.0 Mux TS3USB221ARSER P.44
USB 2.0

WLAN+BT M.2
PCIe x1
CNVi

RJ45
Transformer iG/2.5G
LOM 1G Lan Realtek RTL8111 H
PCIe x1

M.2 SSD1 PCIe
PCIe x4 Gen4

Intel CPU
ADL-P
45W

USB3.2 Gen1
USB2.0
USB3.2 Type-A CONN
USB2.0
USB2.0 Type-A CONN
USB2.0
USB2.0 Type-A CONN

USB2.0
KB Controller PWM Driver
KSI/KSO
SPI ROM 32MB
PWM LED
KSI/KSO
PWM LED
4 Zone KB
I2C To EC
I2C

USB2.0
ELC STM32F070CBT6TR
I2C
Front Light

USB2.0
HD Camera
DMIC

HDA
Audio Codec ALC3254
Audio Jack
Speaker

BIOS SPI ROM 32MB
SPI(G3 mode)
Touch Pad
I2C
PS2
FAN
FAN
PWM
NPCX99ND
12CH
KB Matrix
Thermal Sensor F75399M+G788P81U
SMBus
Charger
Battery

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Board ID table

Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10K	3.000	Pre-EVT
2	100	17.8K	2.801	EVT
3	100	27K	2.598	
4	100	37.4K	2.402	DVT1
5	100	49.9K	2.201	DVT2
6	100	64.9K	2.001	
7	100	82.5K	1.808	Pilot
8	100	107K	1.594	
9	100	154K	1.299	
10	100	200K	1.1	

Power State

SIGNAL / STATE	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCH SMBUS Address Table

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PCH_SMBUS Port	Power Rail	Device	Address
PCH_SMBCLK PCH_SMBDATA	+3VALW_PCH	JDIMM1	
		JDIMM2	

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address
GPU_THM_SMBCLK GPU_THM_SMBDAT	+3VS		
		Thermal 1	0x98h
		Thermal 2	0x9Ah
		GPU (GN20E)	0x9E
PBAT_CHG_SMBCLK PBAT_CHG_SMBDAT	+3VALW_EC	BAT	0x16
		CHGR	0x12
DAT_TP_SIO_I2C_CLK CLK_TP_SIO_I2C_DAT	+TP_VDD	Touch Pad	0x2C
UPD1_SMBCLK UPD1_SMBDAT	+3V_VSYS	CCG6SF	0x08

TGL-H-PCH H510

HSIO	USB3.2	PCIe	SATA3	Function
0	1			JUSB1
1	2			
2	3			JUSB (DB)
3	4			JUSB (DB)
4	5			
5	6			
6	7			
7	8			
8				
9				
10				
11				
12		7		
13				
14		9		JSSD2 , 2280 SATA x2 / PCIe x4
15		10		
16		11	0A	
17		12	1A	
18		13	0B	
19		14	1B	LAN
20		15		WLAN
21		16		
22		17		
23		18		
24		19		
25		20		
26		21		
27		22		
28		23		
29		24		

USB2	Function
1	JUSB1
2	
3	JUSB (DB)
4	JUSB (DB)
5	HD CAM
6	Type C
7	ELC MCU
8	4Zone MCU
9	
10	
11	
12	
13	
14	Bluetooth

TGL-H-CPU

PCIE4	Function
0	JSSD1 , 2280 PCIe x4 (GEN4)
1	
2	
3	
TCP0	Function
0	CPU side Type C
1	

Symbol Note :

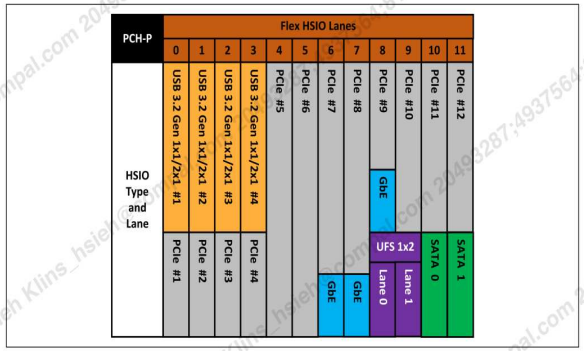
Digital Ground

Analog Ground

60 mils/1A = 1/3 oz
40 mils/1A = 0.5 oz
20 mils/1A = 1 oz
10 mils/1A = 2 oz

1.3.1 PCH-P

Figure 1. Flexible HSIO Lane Multiplexing in PCH-P



Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
+12.6V_BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCCIN	CPU FIVR input power supply	ON	OFF	OFF	OFF	OFF
+VCCIN_AUX	PCH FIVR input power supply	ON	OFF	OFF	OFF	OFF
+VCCIN_AUX_PCH	PCH power supply	ON	OFF	OFF	OFF	OFF
+3.3V_BAT_LDO	RTC power	ON	ON	ON	ON	ON
+RTC_CELL	+3.3V_BAT_LDO/+3VLP for suspend power	ON	ON	ON	ON	ON
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW_PCH	+3VALW Primary Power Well for PCH	ON	ON	ON	ON*	OFF
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+1.8V_PRIM	System +1.8V power rail	ON	ON	ON	ON*	OFF
+1.05VO_OUT_FET	System +1.05V power rail	ON	ON	ON	ON*	OFF
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	ON	OFF	ON
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+2.5V_MEM	DDR4 +2.5Vpp power rail	ON	ON	ON	OFF	ON
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF	OFF
+1.05V_VCCSTG	Gated version of VCCST	ON	OFF	OFF	OFF	OFF
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+1.8V_RUN	System +1.8VS power rail	ON	ON	OFF	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

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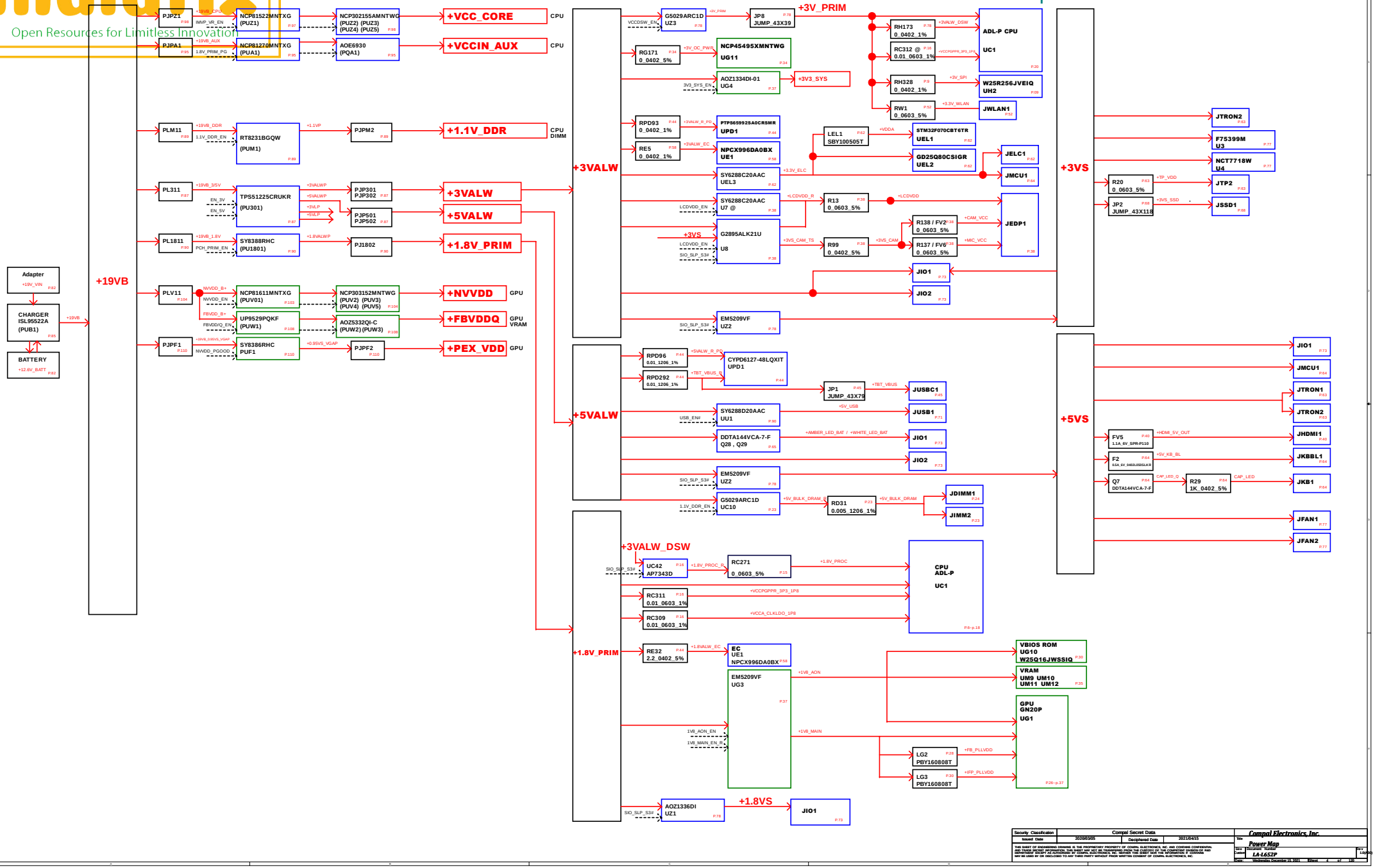

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Power Sequence
G3 -> S0

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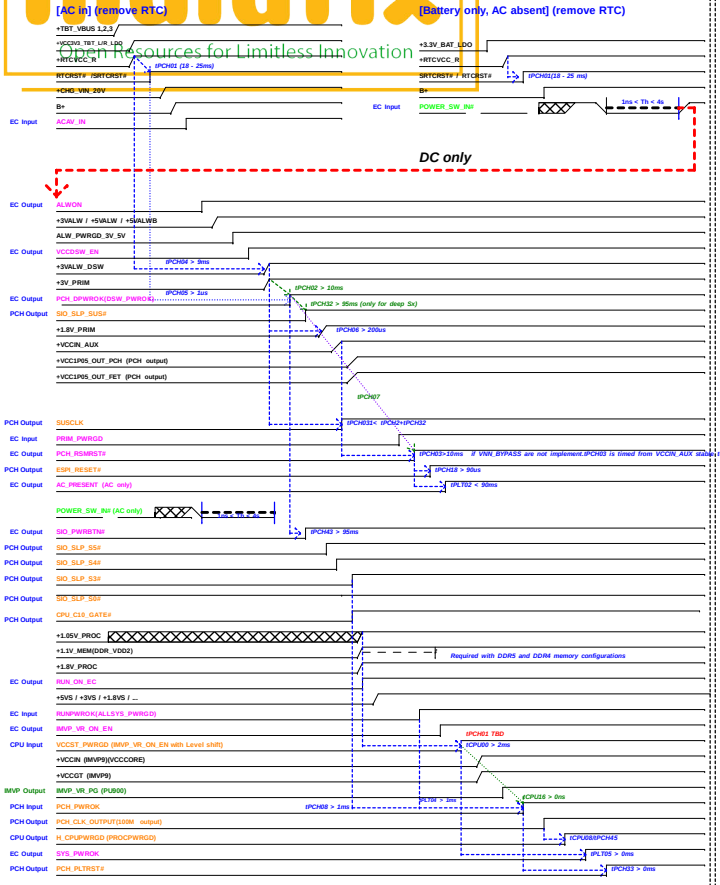
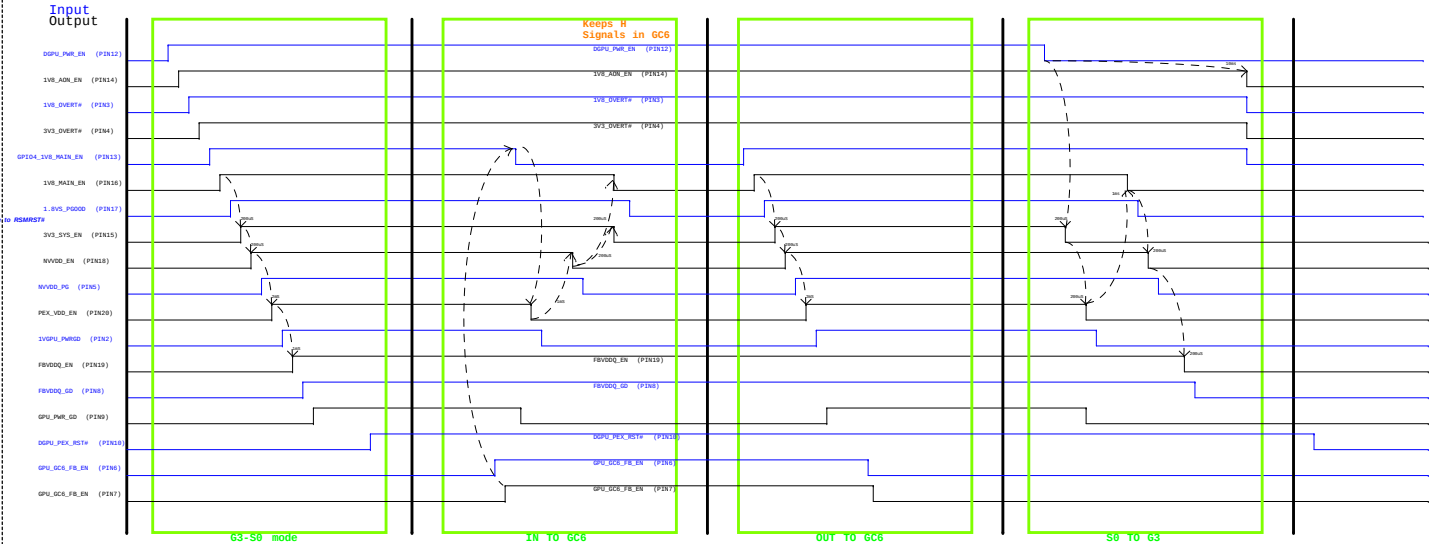


Original power seuence is copied from Tributo ADLP

Modification
1. CPU_C10_GATE goes high earlier than VCCSTG(Need to check Modenat TGL power sequence report)
2. Add VCC1P8A signal
3. Net name need to aligened with Fiorano TGL-H

GPU squence



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ES CPU I5 CPU I7 QS CPU I5 CPU I7 Pilot CPU I5 CPU I7

UC1 FJ80715047587817 QXZR J0 1G S QVW4R3@ SA0000EFW0L
UC1 FJ80715047587821 QY0Z J0 1.2G S QVW8R3@ SA0000EFN0L
UC1 FJ80715047585803 QYY1 K0 2.5G S QVW10R3@ SA0000F4F0L
UC1 FJ80715047586105 QYY4 K0 2.3G S QVW8R3@ SA0000F2X1L
UC1 FJ80715047585804 SRLCY L0 2.5G A31 ! 6@ SA0000F7F3L
UC1 FJ80715047586106 SRLD1 L0 2.3G A31 ! I7@ SA0000F7I3L

follow E board

+3V_PRIM
RC3 1 2 100K_0201_5% KB_DET#
RC6 1 2 10K_0201_5% USB_OC1#
RC7 1 2 10K_0201_5% USB_OC2#

eDP

UC1A
REV 0.6
ADL-P_BGA1744

<39> EDP_TXP3 W3 DDIA_TXP_3
<39> EDP_TXN3 AA3 DDIA_TXN_3
<39> EDP_TXP2 AA1 DDIA_TXP_2
<39> EDP_TXN2 AB1 DDIA_TXN_2
<39> EDP_TXP1 AB3 DDIA_TXP_1
<39> EDP_TXN1 AD3 DDIA_TXN_1
<39> EDP_TXP0 AF1 DDIA_TXP_0
<39> EDP_TXN0 AD1 DDIA_TXN_0
<39> EDP_AUXP AF3 DDIA_AUXP
<39> EDP_AUXN AG3 DDIA_AUXN
PCH_E22_AUX_P ER23 GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD
PCH_E23_AUX_N ET23 GPP_E23/DDPA_CTRLDATA
<39> EDP_HPD EV25 GPP_E14/DDSP_HPDA/DISP_MISC_A
RC9 100K_0201_5%
AP6 DDIB_TXP_3
AP8 DDIB_TXN_3
AM6 DDIB_TXP_2
AM8 DDIB_TXN_2
AK6 DDIB_TXP_1
AK8 DDIB_TXN_1
AH6 DDIB_TXP_0
AH8 DDIB_TXN_0
AE6 DDIB_AUXP
AE8 DDIB_AUXN
EK46 GPP_H15/DDPB_CTRLCLK/PCIE_LINK_DOWN
EL46 GPP_H17/DDPB_CTRLDATA
EB47 GPP_A18/DDSP_HPDB/DISP_MISCB
DV54 GPP_A21/DDPC_CTRLCLK
DV52 GPP_A22/DDPC_CTRLDATA
<64> KB_DET#
TP@ PAD-D TH50 TBT_0_LSX_TX TBT_0_LSX_RX ER26 ET26 GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD/BSSB_LS0_RX GPP_E19/DDP1_CTRLDAT/TBT_LSX0_RXD/BSSB_LS0_TX Strap_Pin
TP@ PAD-D TH51 TBT_1_LSX_TX_STRAP TBT_1_LSX_RX_STRAP EL26 EN26 GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD/BSSB_LS1_RX GPP_E21/DDP2_CTRLDAT/TBT_LSX1_RXD/BSSB_LS1_TX Strap_Pin
<9> GPU_ID1 TBT_2_LSX_RX_STRAP FC37 EV37 GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/BSSB_LS2_RX/GSPI2_CS0# GPP_D10/ISH_SPI_CLK/DDP3_CTRLDAT/TBT_LSX2_RXD/BSSB_LS2_TX/GSPI2_CLK Strap_Pin
<9> GPU_ID2 TBT_3_LSX_RX_STRAP EY37 FA37 GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/BSSB_LS3_RX/GSPI2_MISO GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDAT/TBT_LSX3_RXD/BSSB_LS3_TX/GSPI2_MOSI Strap_Pin
<44> TCP0_HPD DY54 EB49 GPP_A17/DISP_MISCC EB51 GPP_A19/DDSP_HPD1/DISP_MISC1 GPP_A20/DDSP_HPD2/DISP_MISC2
<73> USB_OC1# USB_OC2# DY47 DY49 GPP_A14/USB_OC1#/DDSP_HPD3/DISP_MISC3 GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4
<38> ENWOD_PCH ET21 VDDEN
<29,39> PCH_EDP_BKOFF# EN21 eDP_BKLTEN
<39> PCH_BKL_PWM EL21 eDP_BKLTCTL
RC1904 100K_0201_5%

By 5/7 modify

need confirm

USB_OC1# : Type-A JIO2 IOR

non TBT Add cap 5/18 modify

TCP0_TXRX_P1 BE8 TBT_0_TRX_DTX_P1 <45>
TCP0_TXRX_N1 BE6 TBT_0_TRX_DTX_N1 <45>
TCP0_TXRX_P0 BG8 TBT_0_TRX_DTX_P0 <45>
TCP0_TXRX_N0 BG6 TBT_0_TRX_DTX_N0 <45>
TCP0_TX_P1 AY3 TBT_0_TTX_DRX_P1 <45>
TCP0_TX_N1 BB3 TBT_0_TTX_DRX_N1 <45>
TCP0_TX_P0 BD3 TBT_0_TTX_DRX_P0 <45>
TCP0_TX_N0 BE3 TBT_0_TTX_DRX_N0 <45>
TCP0_AUX_P BB1 TBT_0_AUXP CT408 2 1 0.1U_0201_10V6K TBT_0_AUXP_C <45>
TCP0_AUX_N BD1 100K_0201_5% 1 2 R6991 PCH_E22_AUX_P
TBT_0_AUXN CT409 2 1 0.1U_0201_10V6K TBT_0_AUXN_C <45>
100K_0201_5% 1 2 R6992 PCH_E23_AUX_N

Type-C (JUSBC1)

TCP1_TXRX_P1 AV8
TCP1_TXRX_N1 AY6
TCP1_TXRX_P0 AY8
TCP1_TXRX_N0 AP3
TCP1_TX_P1 AR3
TCP1_TX_N1 AU3
TCP1_TX_P0 AW3
TCP1_TX_N0 AR1
TCP1_AUX_P AU1
TCP1_AUX_N

TCP2_TXRX_P1 BN8
TCP2_TXRX_N1 BN6
TCP2_TXRX_P0 BL8
TCP2_TXRX_N0 BL6
TCP2_TX_P1 BK3
TCP2_TX_N1 BM3
TCP2_TX_P0 BG3
TCP2_TX_N0 BH3
TCP2_AUX_P BH1
TCP2_AUX_N BK1

TCP3_TXRX_P1 BW8
TCP3_TXRX_N1 BU8
TCP3_TXRX_P0 BU6
TCP3_TXRX_N0 BU3
TCP3_TX_P1 BV3
TCP3_TX_N1 BN3
TCP3_TX_P0 BR3
TCP3_TX_N0 BR1
TCP3_AUX_P BU1
TCP3_AUX_N

VSS AL3 TCRCOMP_DN
TCP_RCOMP AM1
DISP_UTILS_2 AF32 DISP_UTILS_2_TP RC5909 1 2 100K_0201_5%
DDIA_RCOMP AJ1 DDIA_RCOMP RC12 1 2 150_0201_1%
DDIB_RCOMP AL1 DDIB_RCOMP RC385 1 2 150_0201_1%
DISP_UTILS_1 DJ1 DISP_UTILS_1_TP RC5910 1 2 100K_0201_5%
RC10 2.2K_0201_1%

+3V_PRIM
RC13 4.7K_0201_5% TBT_0_LSX_RX RC15 20K_0201_5%
TBT LSX #0 PINS VCCIO CONFIGURATION
Weak Internal Pull down 20k
SAMPLING - RSMRSTB

HIGH	3.3V
LOW	1.8V

RC14 4.7K_0201_5% TBT_1_LSX_RX_STRAP RC16 20K_0201_5%
TBT LSX #1 PINS VCCIO CONFIGURATION
Weak Internal Pull down 20k
SAMPLING - RSMRSTB

HIGH	3.3V
LOW	1.8V

RC213 4.7K_0201_5% TBT_2_LSX_RX_STRAP RC214 20K_0201_5%
TBT LSX #1 PINS VCCIO CONFIGURATION
Weak Internal Pull down 20k
SAMPLING - RSMRSTB

HIGH	3.3V
LOW	1.8V

RC215 4.7K_0201_5% TBT_3_LSX_RX_STRAP RC216 20K_0201_5%
TBT LSX #1 PINS VCCIO CONFIGURATION
Weak Internal Pull down 20k
SAMPLING - RSMRSTB

HIGH	3.3V
LOW	1.8V

PLACE CLOSE TO THE SIGNAL TO AVOID STUB

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TOP SWAP OVERRIDE

GPP_B14 / SPKR (Internal 20 K Pull Down)

0 = Disable "Top Swap" mode. (Default)

1 = Enable "Top Swap" mode.

NO REBOOT

GPP_B18/GSPI0_MOS (Internal 20 K Pull Down)

0 = Disable "No Reboot" mode

1 = Enable "No Reboot" mode (This function is useful when running ITP/XDP).

Reserved

GPP_F7 (Weak internal PD 20K)

Reserved

GPP_F10 (Weak internal PD 20K)

BOOT STRAP 1

GPP_H0 (Weak internal PD 20K)

This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.

BOOT STRAP 2

GPP_H1 (Weak internal PD 20K)

This is bit 2 of a total of 4-bit encoded pin straps for boot configuration.

BOOT STRAP 3

GPP_H2 (Weak internal PD 20K)

This is bit 3 of a total of 4-bit encoded pin straps for boot configuration.

DFXTESTMODE(ITP_PMODE)

DBG_PMODE (Internal 20 K Pull UP)

0 = DFXTESTMODE ENABLED

1 = DFXTESTMODE DISABLED(DEFAULT)

CPU_EAR

```
Stall CPU reset sequence until de-asserted:
- 1 = (Default) Normal Operation; No stall.
- 0 = Stall
```

The ADL-P processor supports the configurations shown in the following tables:

Table 54. PCI Express* 8 - Lane Reversal Mapping

Bifurcation	Link Width		CFG Signals			Lanes							
	0:1:0	0:1:1	CFG [6]	CFG [5]	CFG [4]	0	1	2	3	4	5	6	7
PCIe controller						PCIe 010							
1x8	x8	N/A	1	1	1	0	1	2	3	4	5	6	7
1x8 **Reversed**	x8	N/A	1	1	0	7	6	5	4	3	2	1	0

Notes: 1. For CFG bus details, refer to Reset and Miscellaneous Signals on page 144.
2. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
3. For reversal lanes, for example: When using 1x4, the 4 lane device should use lanes 4:7, so lane 7 will be connected to lane 0 of the Device.

Table 56. ADL P PCI Express* 4 - Lane Reversal Mapping

Bifurcation	Link Width	CFG Signals	Lanes			
	0:6:0	CFG [14]	0	1	2	3
PCIe controller			PCIe 060			
1x4	x4	1	0	1	2	3
1x4 **Reversed**	x4	0	3	2	1	0
PCIe controller						PCIe 062
1x4	x4	1	0	1	2	3
1x4 **Reversed**	x4	0	3	2	1	0

11.4 Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[17:0]	Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • CFG[3:0]: Reserved configuration lanes. • CFG[4]: eDP enable: — 1 = Disabled. — 0 = Enabled. • CFG[6:5]: Reserved configuration lanes. • CFG[7]: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • CFG[13:8]: Reserved configuration lanes. • CFG[14]: PEG60 Lane Reversal: — 1 = (Default) Normal — 0 = Reversed • CFG[17:15]: Reserved configuration lanes.	I	GTL	SE	S-Processor Line P-Processor Line

Reserve GPIO pin with Prim power for debug

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Issued Date	2020/10/15	Deciphered Date	2021/04/15

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Compal Electronics, Inc.			
Title	P007 - ADL-P(2/13)MISC,MIPI60		
Size	Document Number		Rev
	LA-L652P		1.0(A00)
Date:	Wednesday, December 15, 2021	Sheet	7 of 120

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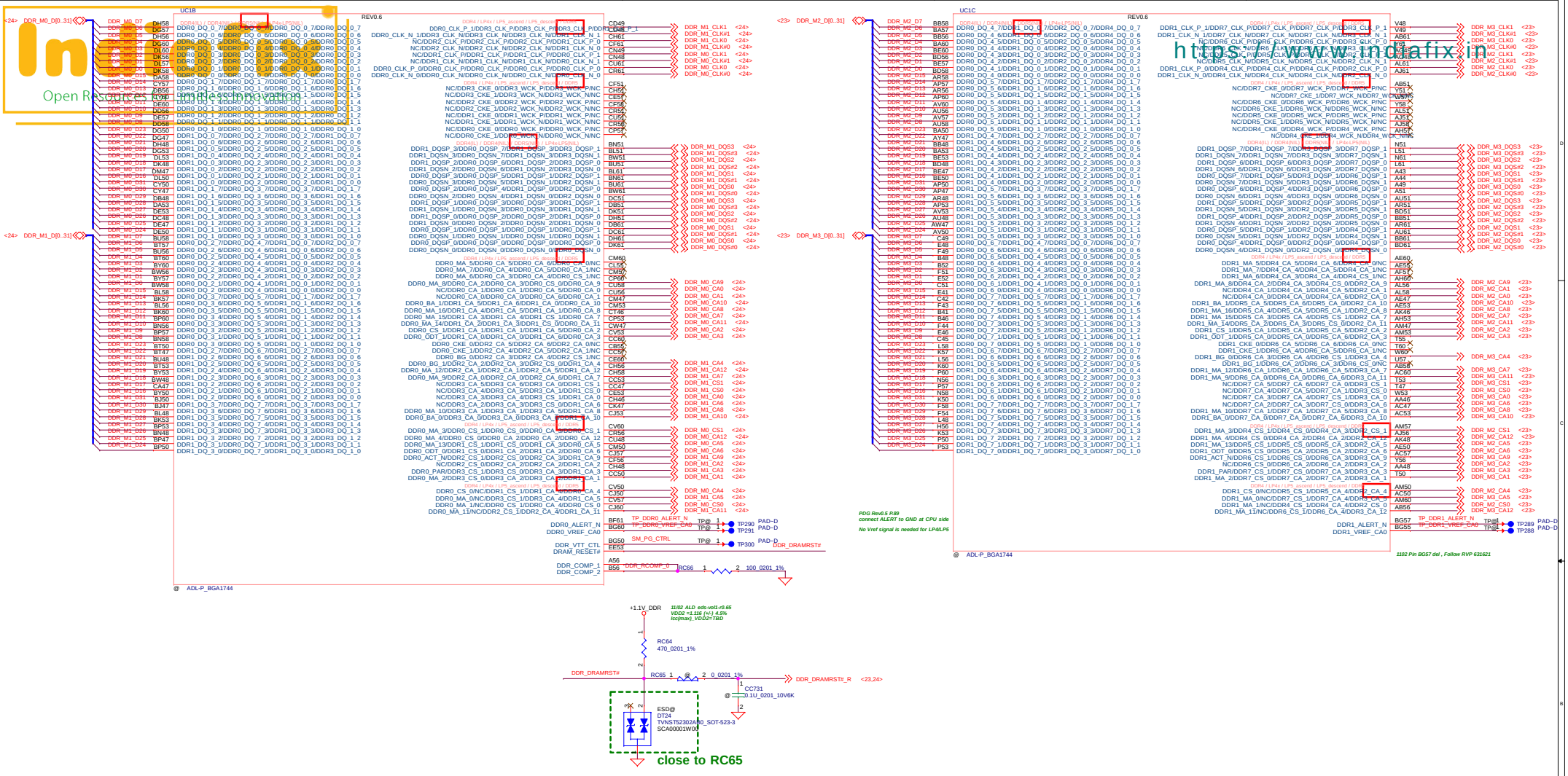

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Security Classification	Compal Secret Data		
Issued Date	2020/09/18	Deciphered Date	2021/04/15

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Compal Electronics, Inc.

Title: **P008 - ADL-P(3/13)LPDDR4/x**

Size	Document Number	Rev
	LA-L652P	1.0(A00)

Date: Wednesday, December 15, 2021 | Sheet 8 of 120

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by 5/17 update for EE

JTAG ODT disable

GPP_E6 (External pull-up is required)
0: JTAG ODT disable
1: JTAG ODT enable
This strap does not have an internal pull-up or pull-down.
External pull-up is recommended

BOOT HALT

SPI0_MOSI(NO INTERNAL PU/PD)
0 = Enable
1 = Disable

CPUNSSC CLOCK FREQ

GPP_B23 (Weak internal PD 20K)
0 = 38.4 MHz clock direct from crystal (default)
1 = 19.2 MHz clock from divider (Device from 38.4MHz crystal)

TLS CONFIDENTIALITY

GPP_C2 (Internal PD 20K)
0 = TLS CONFIDENTIALITY DISABLE
1 = TLS CONFIDENTIALITY ENABLE

CONSENT STRAP

SPI0_IO2(NO INTERNAL PU/PD)
0 = Enable
1 = Disable
PLACE RC115 AND RC122 CLOSE TO THE SPI SIGNAL TO AVOID STUB

A0 PERSONALITY STRAP

SPI0_IO3
0 = Enable
1 = Disable
PLACE RC116 AND RC123 CLOSE TO THE SPI SIGNAL TO AVOID STUB

Boot Strap 0

GPP_C5 (Weak internal PD 20K)
0 = Enable eSPI. (Default)
1 = Disable eSPI.
This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively).
0000 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI enable<--use this
0010 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is disabled
0100 = BIOS on eSPI Peripheral Channel. CSME on master attached SPI.
1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device).
1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI.
Others: Reserved.

SPI ROM

UC1E
REV0.6
ADL-P_BGA1744

SODIMM-1,SODIMM2

1104 Follow RVP 631621 ver.0.7
DDR SMB DAT/CLK connect to EL38,EK38

PD_L&PD_R

ESPI 1.8V

RC95 within 500 mil

eSPI Alert 0 (Server Only):Alert signal from eSPI slave to the PCH.
Note: If only a single Slave is connected, the eSPI Compatibility Specification requires that the Slave must operate with in-band Alert# signaling in order to free up the GPIO pin required for the discrete Alert# pin.
*****Need confirm***
PCH EDS P.72 rev0p7

5/18 by EE modify (PCH_PANEL_GSYNC_DET#)

close to UC1

GPU_ID	GPU_ID1 (AV18)	GPU_ID2 (AW18)	PROJECT_ID1 (ET33)
GN20-E3	L	L	H
GN20-E6	H	H	H
GN20-E8	L	H	H
GN20-P0	H	L	L
GN20-P1	L	L	L

	PROJECT_ID2
AXIOM	H
SIFMLK	L

Footprint co-lay

SPI ROM 32M Byte, support RPMC
W25R256JVEIQ_WSON8_8X6
SA0000D4D00

ROM Socket
ACES_50950-0084N-001_ROM
SP07001QV00

5/10 by EMI modify

1119 Follow Fiorano TGLH add level shift to prevent leakage

RC482 reserve For EC Auto Load Code

close to UC1

junction point to UH 2 each length < 500 mil

RES VALUE = 0 ohm for 1.8V and 3.3V

To SPI ROM
RES VALUE = 15 ohm for 1.8V; 15 ohm for 3.3V,
(SPI0_CLK, SPI0_MSIO, SPI0_MOSI)
33 ohm for 1.8V; 50 ohm for 3.3V,
(SPI0_IO2, SPI0_IO3)

to EC
RES VALUE = 50 ohm for 1.8V; 100 ohm for 3.3V,
(SPI0_CLK, SPI0_MSIO, SPI0_MOSI)
50 ohm for 1.8V; 50 ohm for 3.3V,
(SPI0_IO2, SPI0_IO3)

From MIPI60

SPI0 EC G3 Flash Sharing Topology
Ref 607872_TGL_UP3_PDG_Rev1p1
2-Load Branch Topology (Device Down) with EC Wired-OR Flash Sharing and TPM

PCH — 0-ohm — 15/50-ohm — SPI ROM
100/50-ohm — EC

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Issued Date	2020/10/15	Deciphered Date 2021/04/15

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Compal Electronics, Inc.
Title: P009 - ADL-P(4/13)SPI,SMB,ESPI
Size: LA-L652P
Document Number
Rev: 1.0(A00)
Date: Wednesday, December 15, 2021
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Need to check

UC1F
REV0.6
GPP_H11/UART0_TXD/M2_SKT2_CFG1
GPP_H10/UART0_RXD/M2_SKT2_CFG0
GPP_H13/I2C7_SCL/UART0_CTS#/M2_SKT2_CFG3/ISH_GP7B/DEVSLP1B
GPP_H12/I2C7_SDA/UART0_RTS#/M2_SKT2_CFG2/ISH_GP6B/DEVSLP0B
GPP_D18/UART1_TXD/ISH_UART1_TXD
GPP_D17/UART1_RXD/ISH_UART1_RXD
GPP_H5/I2C0_SCL
GPP_H4/I2C0_SDA
GPP_H7/I2C1_SCL
GPP_H6/I2C1_SDA
GPP_B6/ISH_I2C0_SCL/I2C2_SCL
GPP_B5/ISH_I2C0_SDA/I2C2_SDA
GPP_B8/ISH_I2C1_SCL/I2C3_SCL
GPP_B7/ISH_I2C1_SDA/I2C3_SDA
GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
GPP_H8/I2C4_SDA/CNV_MFUART2_RXD
GPP_B17/I2C5_SCL/ISH_I2C2_SCL
GPP_B16/I2C5_SDA/ISH_I2C2_SDA
GPP_D14/ISH_UART0_TXD/I2C4B_SCL
GPP_D13/ISH_UART0_RXD/I2C4B_SDA
GPP_D16/ISH_UART0_CTS#/I2C7B_SCL
GPP_D15/ISH_UART0_RTS#/I2C7B_SDA
GPP_D3/ISH_GP3/BK3/SBK3
GPP_D2/ISH_GP2/BK2/SBK2
GPP_D1/ISH_GP1/BK1/SBK1
GPP_D0/ISH_GP0/BK0/SBK0
GPPC_RCOMP
@ ADL-P_BGA1744

Fiorano ADL-P
ISH_GP0 for KB Acc INT#
ISH_GP1 for Hinge Acc INT#
ISH_GP2 for NC
ISH_GP3 for ALS INT#
ISH_GP4 for ECI INT#
ISH_GP5 for USB_OC3#
ISH_GP6 for SPKR strap pin
ISH_GP7 for P-Sensor INT#

1210 ISH_I2C0 /ISH_I2C1 Follow Fiorano ADL-P use 3.3V
PU +3VS at CPU side
ALS+ACC1 (KB)

1229 Reserve ISH_ECI2_INT# with Prim power for debug

DIMM TYPE

1 : Interleave

0 : Non-Interleave

The signal has a weak internal pull-down.

FLASH DESCRIPTOR SECURITY OVERRIDE

GPP_R2/HDA_SDO (Internal 20 K Pull Down)

0 = ENABLE (DEFAULT)

1 = DISABLE (ME can update)

1228 need check follow Fiorano T6LH or CSLP

1119 Reference Fiorano T6LH ,Connect HDA signal

UC1G
REV0.6
GPIO R group 3.3V
GPP_R0/HDA_BCLK/I2S0_SCLK/DMIC_CLK_B0/HDAPROC_BCLK
GPP_R1/HDA_SYNC/I2S0_SFRM/DMIC_CLK_B1
GPP_R2/HDA_SDO/I2S0_TXD/HDAPROC_SDO
GPP_R3/HDA_SDI0/I2S0_RXD/HDAPROC_SDI
GPP_R4/HDA_RST#/I2S2_SCLK/DMIC_CLK_A0
GPP_R5/HDA_SDI1/I2S2_SFRM/DMIC_DATA0
GPP_R6/I2S2_TXD/DMIC_CLK_A1
GPP_R7/I2S2_RXD/DMIC_DATA1
GPP_D19/I2S_MCLK1_OUT
GPP_S0/SNDW0_CLK/I2S1_SCLK
GPP_S1/SNDW0_DATA/I2S1_SFRM
GPP_S2/SNDW1_CLK/DMIC_CKL_A0/I2S1_TXD
GPP_S3/SNDW1_DATA/DMIC_DATA0/I2S1_RXD
GPP_S4/SNDW2_CLK/DMIC_CLK_B0
GPP_S5/SNDW2_DATA/DMIC_CLK_B1
GPP_S6/SNDW3_CLK/DMIC_CLK_A1
GPP_S7/SNDW3_DATA/DMIC_DATA1
GPP_A11/PMC_I2C_SDA
GPP_A13/PMC_I2C_SCL
SNDW_RCOMP_1
SNDW_RCOMP_2
@ ADL-P_BGA1744

Reserve for DMIC

5/5b add

Close to RC5886

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Title: P010 - ADL-P(5/13)HDA,I2C,ISH

Size: Document Number: LA-L652P

Rev: 1.0(A00)

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STRAP FOR SPI 1.8V/3.3V SEL

SPIVCCIOSEL

0 = SPI voltage is 3.3V (4.7 k pull-down to GND)

1 = SPI voltage is 1.8V (4.7K pull-up to DSW_PWROK)

+3VALW_DSW

RC2411 2 4.7K_0201_5% SPIVCCIOSEL_STRAP

RC2461 2 4.7K_0201_5%

Reserved

Weak Internal PD 20k.
This strap should sample LOW. There should NOT be any on-
board device driving it to opposite direction during strap sampling.

+3VALW_DSW

@RC2401 2 4.7K_0201_5% GPD7_STRAP

@RC3681 2 20K_0201_5%

X00_43:Customer request Reference CSLP
PCIE:CR 7->4
PCIE:WLAN 8->12
PCIE CLK:WLAN 2->3
PCIE CLK:CR 1->2
PCIE CLK:SSD 3->0
PCIE CLK:GPU 0->3

UC1K

REV0.6

Gen4 DP1 DP0 CLKOUT_PCIE_P6
CLKOUT_PCIE_N6
DU5 DU6 CLKOUT_PCIE_P5
CLKOUT_PCIE_N5
DP5 DP6 CLKOUT_PCIE_P4
CLKOUT_PCIE_N4/UFS_REF_CLK

Gen4 DN10 DN11 CLKOUT_PCIE_P3
CLKOUT_PCIE_N3
DR4 DR6 CLKOUT_PCIE_P2
CLKOUT_PCIE_N2
DU1 DU3 CLKOUT_PCIE_P1
CLKOUT_PCIE_N1
Gen5 DT10 DT11 CLKOUT_PCIE_P0
CLKOUT_PCIE_N0
DJ3 XCLK_BIASREF

Gen5 PEG
LAN
Gen2 WLAN
Gen4 SSD1

<26> CLK_PEG_P3
<26> CLK_PEG_N3
<73> CLK_PCIE_P2
<73> CLK_PCIE_N2
<52> CLK_PCIE_P1
<52> CLK_PCIE_N1
<68> CLK_PCIE_P0
<68> CLK_PCIE_N0

RC205 1 2 60.4_0201_1% XCLK_BIASREF

GPP_A12/SATAXPCIE1/SATAGP1/SRCCLKREQ9B#
GPP_E0/SATAXPCIE0/SATAGP0/SRCCLKREQ9#
GPP_E16/RSVD_TP/SRCCLKREQ8#
GPP_A8/SRCCLKREQ7#
GPP_F19/SRCCLKREQ6#
GPP_H23/SRCCLKREQ5#
GPP_H19/SRCCLKREQ4#
GPP_D8/SRCCLKREQ3#
GPP_D7/SRCCLKREQ2#
GPP_D6/SRCCLKREQ1#
GPP_D5/SRCCLKREQ0#

DY46
EY22
EY22
EB54
EF31
ET43
ER46
FC34 CLKREQ_PCIE#3_R
FC31 CLKREQ_PCIE#2_R
FB36 CLKREQ_PCIE#1_R
FB29 CLKREQ_PCIE#0_R

RC196 1 0ohm 2 0_0201_5%
RC306 1 0ohm 2 0_0201_5%
RC191 1 0ohm 2 0_0201_5%
RC200 1 0ohm 2 0_0201_5%

SPK_ID1 <73>
SPK_ID2 <73>
PCH_4ZONE_KB_DET# <64>
OD_EN <38>

CLKREQ_PCIE#3 <26> <-Gen5 PEG
CLKREQ_PCIE#2 <73> <-Gen2 LAN
CLKREQ_PCIE#1 <52> <-Gen2 WLAN
CLKREQ_PCIE#0 <68> <-Gen4 SSD1

XTAL_OUT
XTAL_IN
EJ61
GPD8/SUSCLK
EVS8 XTAL_PCH_38P4M_IN
EVS8 XTAL_PCH_38P4M_IN
EJ61 SUSCLK
EVS8 PCH_RTCX2
EVS6 PCH_RTCX1
RTCX2
RTCX1
FA55 PCH_RTCRST#
FB56 SRTCRST#
RTCRST#
SRTCRST#
EBS2
EW25
GPP_A7/SRCCLK_OE#
GPP_E15/RSVD_TP/SRCCLK_OE#

SUSCLK RH208 1 @ 2 0_0201_1% SUSCLK_EC <58>
RH209 1 @ 2 0_0201_1% SUSCLK_WLAN <52>

PAD-D 1 TP@ TP307

@ ADL-P_BGA1744

0111 TBD

XTAL_PCH_38P4M_IN RC186 0_0201_5% XTAL_PCH_38P4M_IN CC10 10P_0201_50V8
RC202 200K_0201_1% YC1 38.4MHZ_10PF_8Y38420005
XTAL_PCH_38P4M_OUT RC194 0_0201_5% XTAL_PCH_38P4M_OUT CC11 10P_0201_50V8

PCH_RTCX1 RC199 0_0201_5% PCH_RTCX1_R CC12 18P_0201_50V8J
RC201 10M_0201_5% ESR MAX=50k ohm YC2 32.768KHZ_12.5PF_9H03265002
PCH_RTCX2 RC202 0_0201_5% PCH_RTCX2_R CC14 18P_0201_50V8J

PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification
compliant differential output clocks to PCIe* devices
• CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1,Gen2, and Gen3 support
• CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support

+3VS

SUSCLK 1 @ESD@ CC13 0.1U_0201_10V6K 2

CLKREQ_PCIE#3 RC185 2 1 10K_0201_5%
CLKREQ_PCIE#2 RC187 2 1 10K_0201_5%
CLKREQ_PCIE#1 RC188 2 1 10K_0201_5%
CLKREQ_PCIE#0 RC189 2 1 10K_0201_5%

+RTCVCC

@ CLME1 SHORT PADS CC15 1U_0201_6.3V6M
SRTCRST# RC203 20K_0201_5%
PCH_RTCRST# RC206 20K_0201_5%
@ CLCMOS1 SHORT PADS CC16 1U_0201_6.3V6M

PDG_An RC delay circuit with a time delay in the range of 18 - 25 ms should be provided. The circuit should be connected to VCCRTC.

+1.05V_PROC

RC239 1K_0201_5%

VCCST_PWRGD_1.05V RC243 1 @ 2 1K_0201_5% PM_RSMRST_PWRGD_MIP60 <79>
PCH_RSMRST#_AND RC244 1 2 1K_0201_5%

<14> VCCST_PWRGD_TCSS CPU Input, 1.05V RC245 1 @ 2 0_0201_1% VCCST_OVERRIDE_R <78>
VCCST_OVERRIDE RC248 1 @ 2 0_0201_1%
PCH Output, 1.05V

PLACE RC245 and RC248 CLOSE TO MCP - WITHIN 100mils

CPU Type	Config		SYSTEM_ID1	SYSTEMID_2	SYSTEM_ID3
			BID_DIS	XPS or Precision (BID_BC)	P1 or P3 (BID_GPU)
IGFX	XPS	UMA	H	L	L
	Precision	UMA	H	H	L
DGPU	XPS	GN20-P1			
		N20Z-QS1-A1(DVT1)	L	L	L
	Precision	QN20-P1	L	H	H
		QN20-P3			
		N20Z-QS1-A1(DVT1)	L	H	L

+3V_PRIM

RC366 1 2 100K_0201_5%
RC249 1 @ 2 100K_0201_5% SIO_SLP_S0#

+3VALW_DSW

RC1981 2 10K_0201_5% SYS_RESET#

RC2201 2 100K_0201_5% PCH_DPWROK
CC17 1 @ 2 0.01U_0201_16V7

RE61 1 2 100K_0201_5% SYS_PWROK
RC221 1 2 100K_0201_5% PCH_RSMRST#_AND

close to UC1

ESD@ CC27 1 2 100P_0201_50V8J PCH_PWROK
ESD@ CC24 1 2 0.1U_0201_10V6K PCH_PLTRST#
ESD@ CC26 1 2 100P_0201_50V8J VCCST_PWRGD
ESD@ CC25 1 2 100P_0201_50V8J H_CPUPWRGD
ESD@ CC28 1 2 0.1U_0201_10V6K SYS_RESET#

ESD Request:place near CPU side

UC1L

REV0.6

<23,24,78> SIO_SLP_SUS# SIO_SLP_SUS# EN53 SLP_SUS#
<62,79,85> SIO_SLP_S5# SIO_SLP_S5# EG60 GPD10/SLP_S5#
<78,79> SIO_SLP_S4# SIO_SLP_S4# EP56 GPD5/SLP_S4#
<15,38,62,78,79> SIO_SLP_S3# SIO_SLP_S3# EM59 GPD4/SLP_S3#
<79> SIO_SLP_A# SIO_SLP_A# EM57 GPD6/SLP_A#
SIO_SLP_WLAN# EJ57 GPD9/SLP_WLAN#

<79> SIO_SLP_S0# SIO_SLP_S0# DW59 GPP_B12/SLP_S0#
SLP_LAN# EK53 SLP_LAN#

<65,78> PCH_RSMRST#_AND PCH_RSMRST#_AND EH53 RSMRST#
<79> SYS_RESET# SYS_RESET# EK26 SYS_RESET#
<26> PCH_PLTRST# DW57 GPP_B13/PLTRST#

<78> PCH_DPWROK EE48 DSW_PWROK
<58> SYS_PWROK PCH_PWROK EK23 SYS_PWROK
EH51 PCH_PWROK

INTRUDER# DY44 INTRUDER#
SPIVCCIOSEL_STRAP Strap Pin EL53 SPIVCCIOSEL
H_CPUPWRGD BG11 PROCPWRGD

@ ADL-P_BGA1744

GPD3/PWRBTN#
GPD0/BATLOW#
GPD1/ACPRESENT
GPP_B11/PMCALERT#
GPP_H18/PROC_C10_GATE#
GPP_H3/SX_EXIT_HOLDOFF#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7
GPP_E8/SLP_DRAM#
VCCST_PWRGD
VCCST_OVERRIDE
GPP_F20/EXT_PWR_GATE#
GPP_F21/EXT_PWR_GATE2#

EM61 PCH_BATLOW# SIO_PWRBTN# <58,79>
EM56 AC_PRESENT AC_PRESENT <58>
EJ59 I2C2_PD_INT# <44>
EA56 CPU_C10_GATE# PROJECT_ID1 <9>
ER46 PCIE_WAKE# <52,58,68,73>
ET48
ET51
EP58
EJ56
EK60 Strap pin 3.3V GPD7_STRAP
FA22
DJ8 VCCST_PWRGD_CPU RC2321 2 60.4_0201_1% VCCST_PWRGD <78>
DK4 VCCST_OVERRIDE
EH28 EXT_PWR_GATE#_1P8 SLP_DRAM# <78>
EH31 EXT_PWR_GATE2#_1P8

Place RC232 and RC239 close to MCP- WIthin 1.5 inch.

+3VALW_DSW

PCH_BATLOW# RC222 1 2 8.2K_0201_5%
AC_PRESENT RC223 1 2 100K_0201_5%
PCIE_WAKE# RC210 1 2 8.2K_0201_5%
SIO_PWRBTN# RC351 1 2 10K_0201_5%
CPU_C10_GATE# RC372 1 2 100K_0201_5%
SLP_DRAM# RC5908 1 2 100K_0201_5%

+3V_PRIM

PCH_4ZONE_KB_DET# RC5888 1 2 100K_0201_5%
I2C2_PD_INT# RC235 1 2 2.2K_0201_5%
SPK_ID1 100K_0201_5% 2 @ 1 RH48
SPK_ID2 100K_0201_5% 2 1 RH316

+1.8V_PRIM

EXT_PWR_GATE#_1P8 RC667 1 2 75K_0201_1%
EXT_PWR_GATE2#_1P8 RC448 1 2 75K_0201_1%

1119 Dell request Del SYS_RESET# UC29 AND Gate,follow tributo remove it.

+RTC_CELL

INTRUDER# RH329 1 2 1M_0201_5%

PCH GLITCH ISSUE MITIGATION(PDG p.112)

RC225 1 2 100K_0201_5% SIO_SLP_SUS#
CC18 1 @ 2 0.33U_0201_6.3V6M SIO_SLP_S5#
RC237 1 2 100K_0201_5% SIO_SLP_S4#
CC335 1 @ 2 0.33U_0201_6.3V6M
RC227 1 2 100K_0201_5% SIO_SLP_S3#
CC19 1 @ 2 0.33U_0201_6.3V6M
RC229 1 2 100K_0201_5% SIO_SLP_A#
CC21 1 @ 2 0.33U_0201_6.3V6M
RC231 1 2 100K_0201_5% SIO_SLP_WLAN#
CC22 1 @ 2 0.33U_0201_6.3V6M
CC23 1 @ 2 0.33U_0201_6.3V6M SLP_LAN#
RC5905 1 2 100K_0201_5%

+3VS

CC334 0.1U_0201_10V6K

PCH_PLTRST# RC209 100K_0201_5% UC32 MC74VHC1G08P5T5G_SOT-953-5 RC212 100K_0201_5% PCH_PLTRST#_EC <52,68,73,77,79>

+3VS

RC197 1 @ 2 0_0201_1%

RC350 100K_0201_5%

<97> PCH_PWROK_P
<78,97> IMVP_VR_EN

UC31 MC74VHC1G08P5T5G_SOT-953-5 PCH_PWROK RC785 100K_0201_5%

X00_28:Follow CSLP and RVP7.2.

PCH_PWROK DC7 RB521CM-30T2R_SOD923-2 VCCST_PWRGD_PCH_PWROK_DIS RC664 1 2 100_0201_1% SIO_SLP_S3#
VCCST_PWRGD DC8 RB521CM-30T2R_SOD923-2

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Compal Electronics, Inc.

Title: P011 - ADL-P(6/13)CLK,GPIO

Size: Document Number: LA-L652P Rev: 1.0(A00)

Date: Wednesday, December 15, 2021 Sheet 11 of 120

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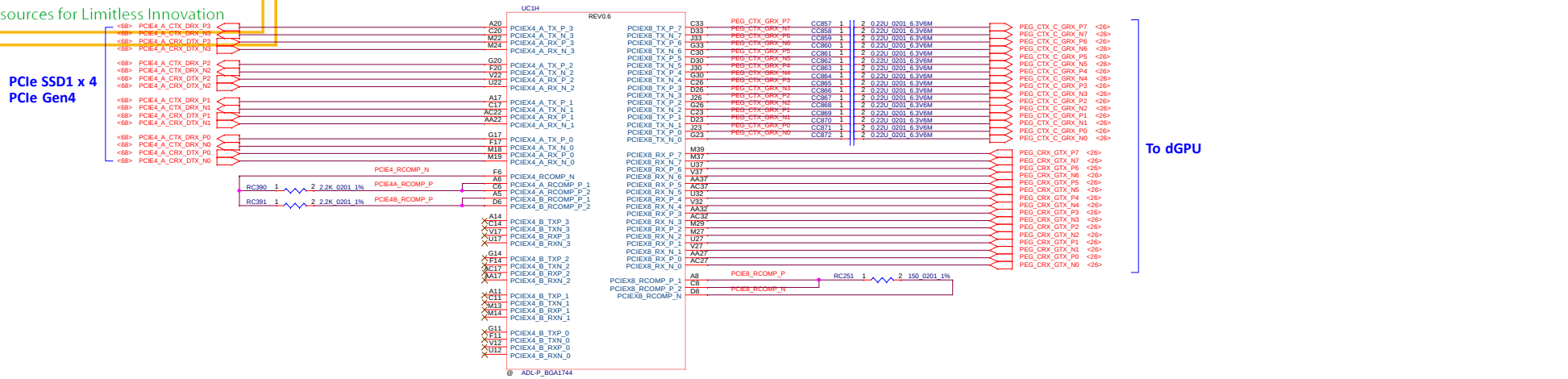

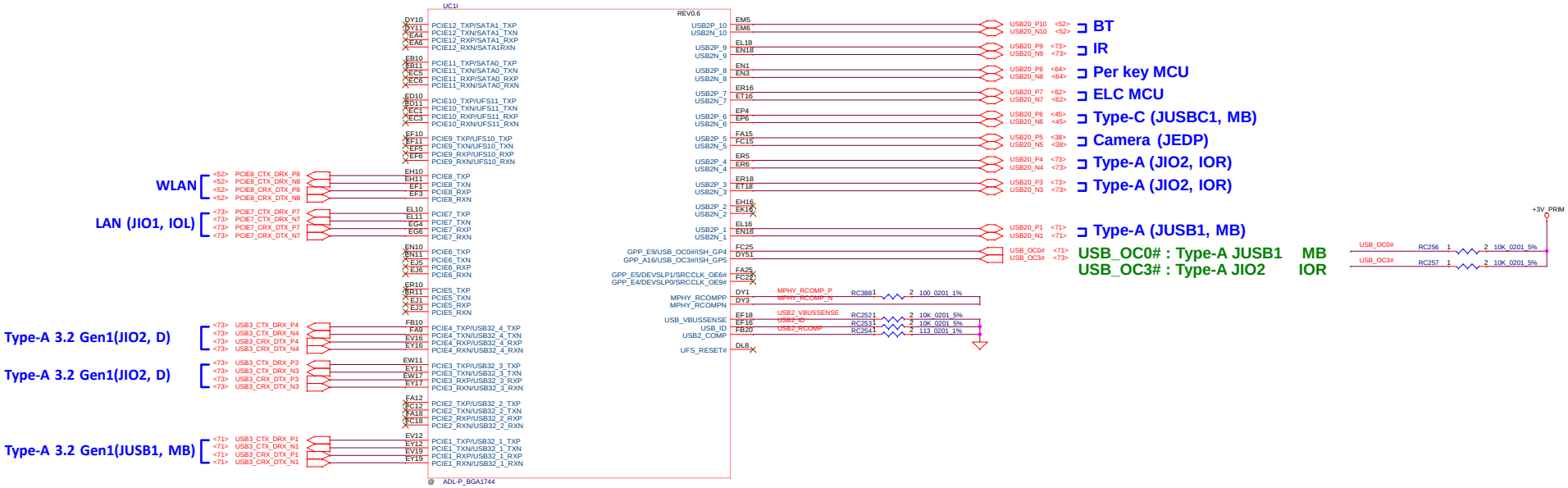

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Compal Electronics, Inc.			
Title	P012 - ADL-P(7/13)PCIE,USB		
Size	Document Number		Rev
	LA-L652P		1.0(A00)
Date:	Wednesday, December 15, 2021	Sheet	12 of 120

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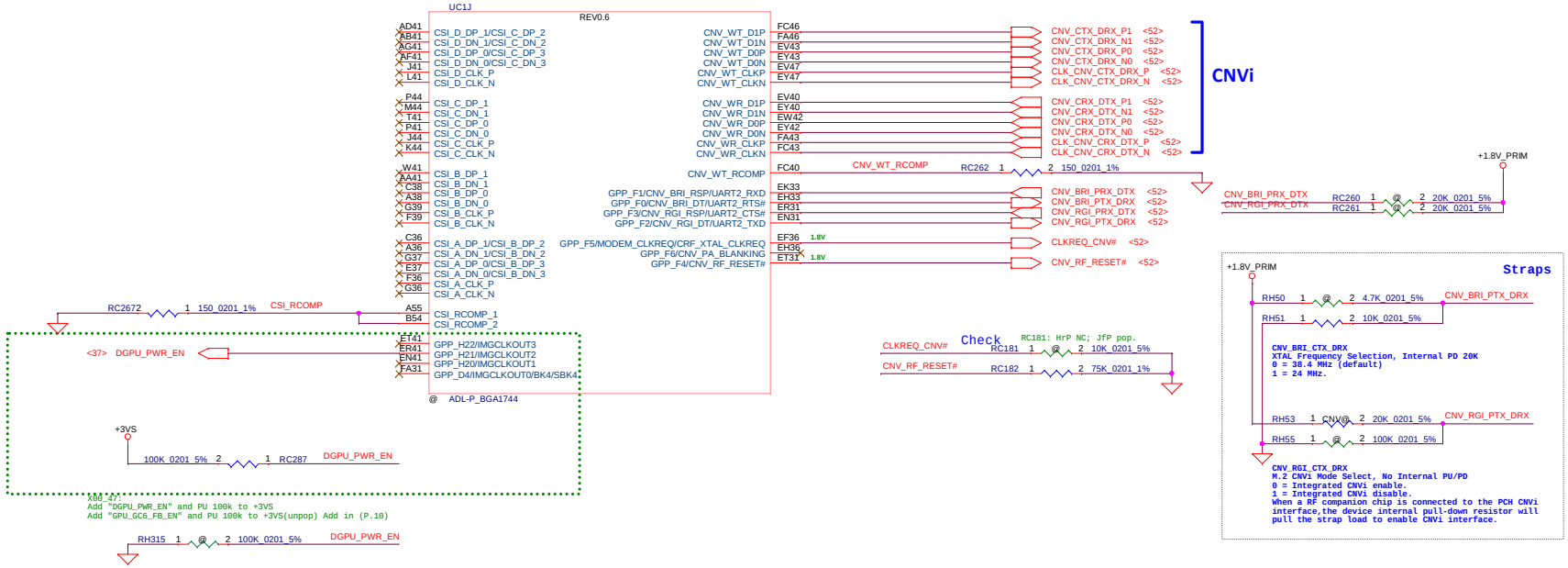

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Compal Electronics, Inc.

Title: **P013 - ADL-P(8/13)CSI,CNVi**

Size	Document Number	Rev
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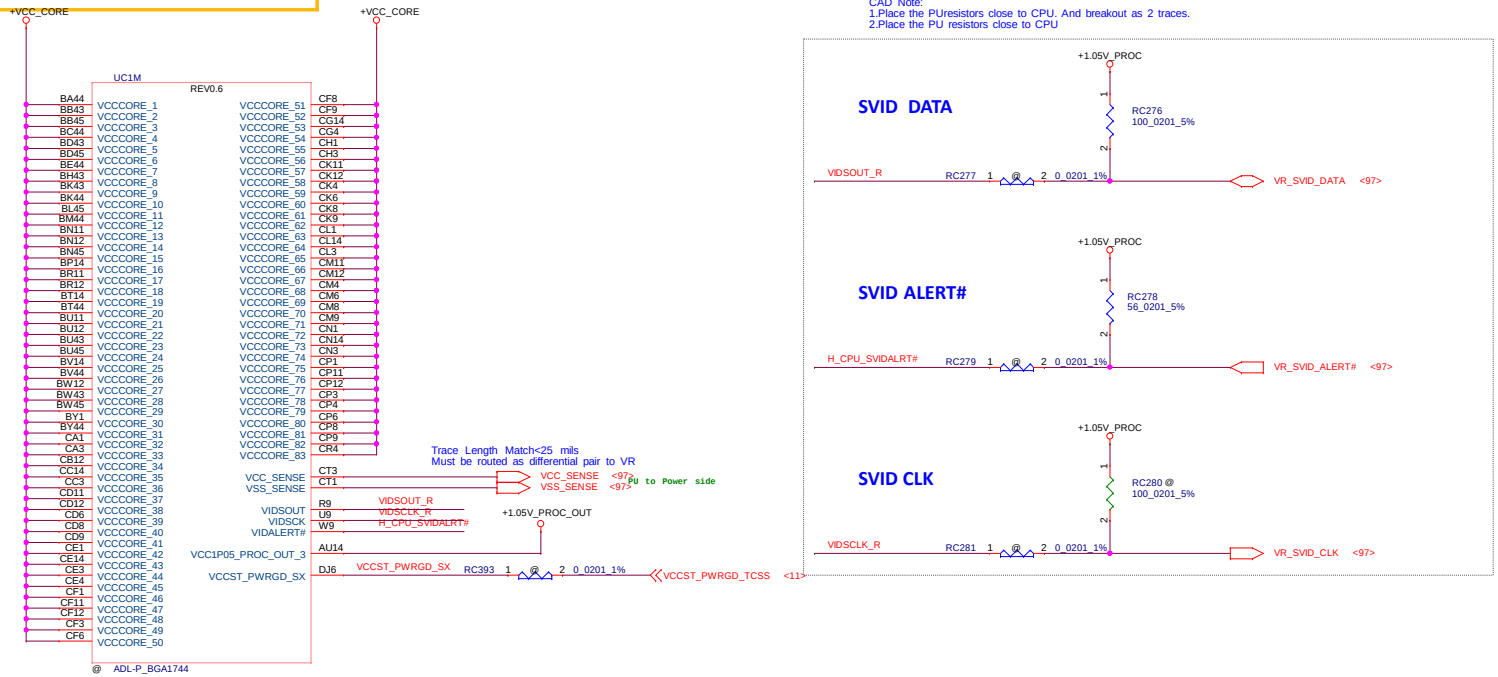
1.Route the Alert signal between the Clock and the Data signals.

CAD Note:
1.Place the PUresistors close to CPU. And breakout as 2 traces.
2.Place the PU resistors close to CPU



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Compal Electronics, Inc.

Title: **P014 - ADL-P(9/13)CPU PWR,SVID**

Size	Document Number	Rev
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5/10 by ESD modify

Secondary Side(BSC)

Secondary Side(BSC)

7/19 by ESD modify

Primary side(TSC)

close to RCC33

11/02 ALD eds-vol1-r0.65
Cap for VDD2 (compal net :+1.1V_DDR)

Primary side Cap
2x 1uF 0402
Secondary Side Cap
4x 1uF 0402
3x 10uF 0402

11/02 ALD eds-vol1-r0.65
VDD2 =1.116 (+/-) 4.5%
Icc(max)_VDD2=TBD

UC1O
REV0.6

1105 Ref PDG627205
Layout notice:
VCC1p8_PROC LDO output to inner BGA pins near AM41 not exceed 10mΩ .

Need to check PDG Output Current

AP7343D-18FS4-7B_X2-DFN1010-5

Follow E Board 0518

1118 RVP 0.81 ,1.8V_PROC enable pin =SLP S3#
5/10a follow Fiorano MLK

TC7SH08FU_SSOP5

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Compal Electronics, Inc.

Title: **P015 - ADL-P(10/13)CPU PWR**

Size: | Document Number: **LA-L652P** | Rev: 1.0(A00)

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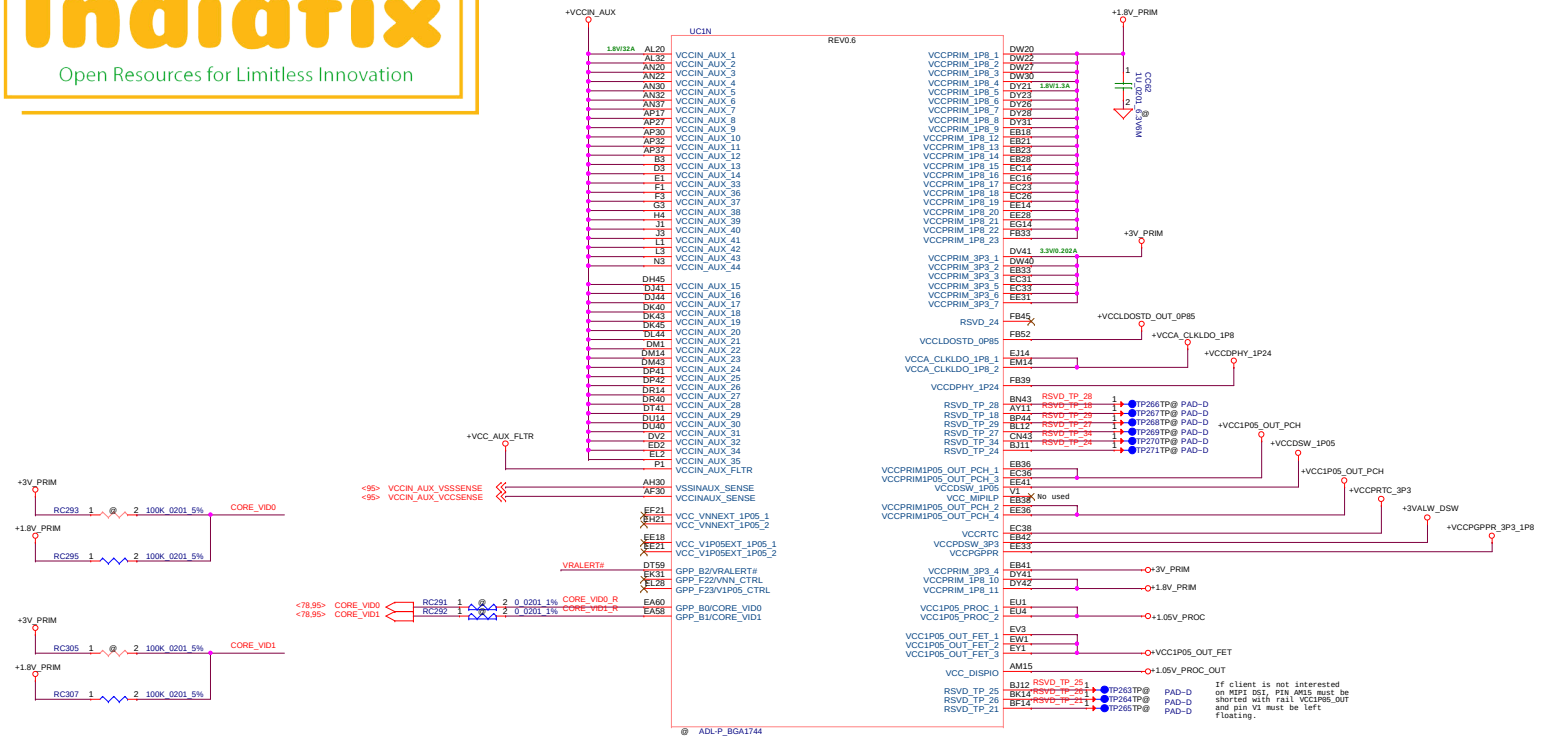
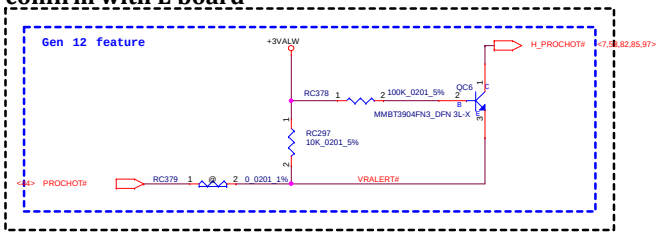
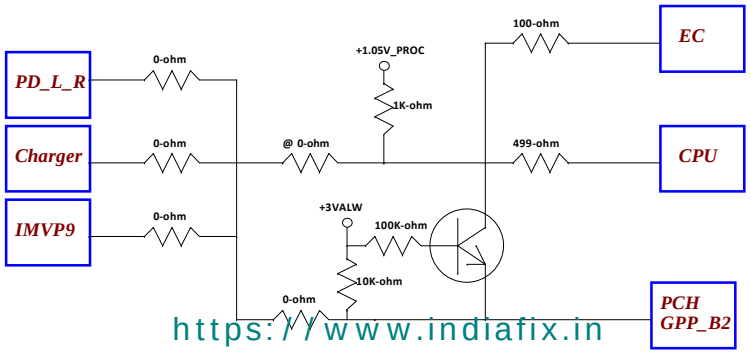
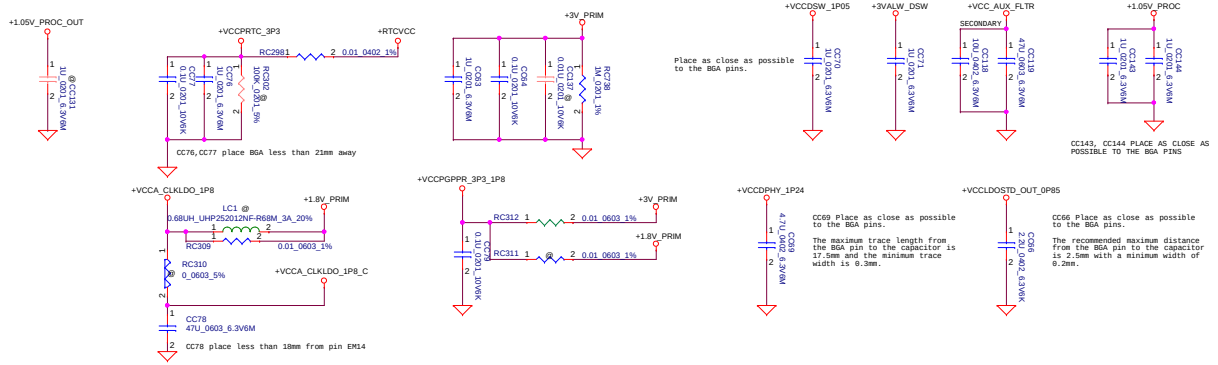


confirm with E board







+VCCA_CLKLDO_1P8
+1.8V_PRIM
LC1 @ 0.68UH_UHP252012NF-R68M_3A_20%
RC309 0.01_0603_1%
RC310 0_0603_5%
+VCCA_CLKLDO_1P8_C
CC78 47U_0603_6.3V6M
CC78 place less than 18mm from pin EM14
+VCCPGPPR_3P3_1P8
+3V_PRIM
RC312 0.01_0603_1%
RC311 0.01_0603_1%
+1.8V_PRIM
+VCCPHY_1P24
CC69 Place as close as possible to the BGA pins.
The maximum trace length from the BGA pin to the capacitor is 17.5mm and the minimum trace width is 0.3mm.
+VCCLDOSTD_OUT_0P85
CC66 Place as close as possible to the BGA pins.
The recommended maximum distance from the BGA pin to the capacitor is 2.5mm with a minimum width of 0.2mm.

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Compal Electronics, Inc.	
Title	P016 - ADL-P(11/13)PCH Power
Size	Document Number: LA-L652P
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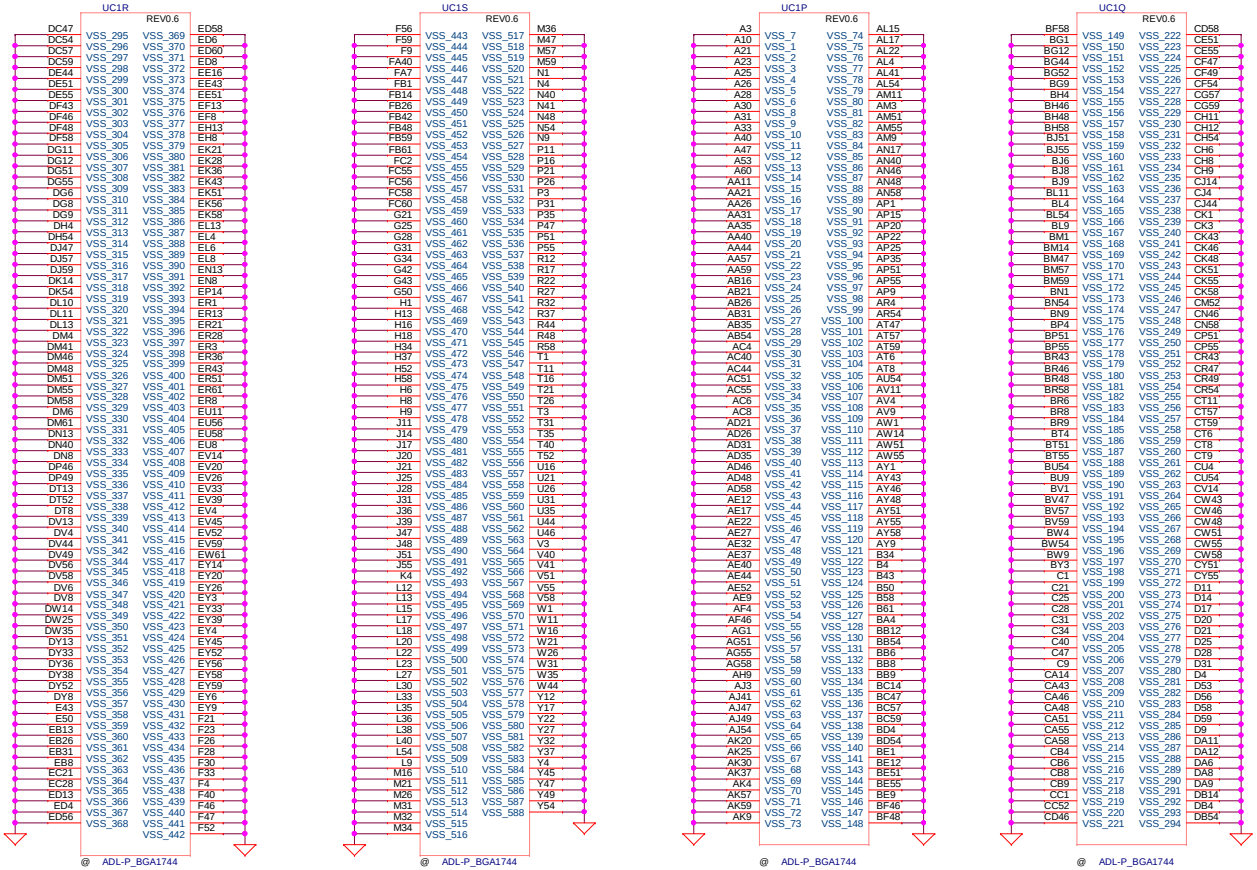
UC1R
REV0.6
DC47 DC54 DC57 DC59 DE44 DE51 DE55 DF43 DF46 DF48 DF58 DG11 DG12 DG51 DG55 DG6 DG8 DG9 DH4 DH54 DJ47 DJ57 DJ59 DK14 DK54 DL10 DL11 DL13 DM4 DM41 DM46 DM48 DM51 DM55 DM58 DN6 DM61 DN13 DN40 DN8 DP46 DP49 DT13 DT52 DT8 DV13 DV4 DV44 DV49 DV56 DV58 DV6 DV8 DW14 DW25 DW35 DY13 DY33 DY36 DY38 DY52 DY8 E43 E50 EB13 EB26 EB31 EB8 EC21 EC28 ED13 ED4 ED56
VSS_295 VSS_296 VSS_297 VSS_298 VSS_299 VSS_300 VSS_301 VSS_302 VSS_303 VSS_304 VSS_305 VSS_306 VSS_307 VSS_308 VSS_309 VSS_310 VSS_311 VSS_312 VSS_313 VSS_314 VSS_315 VSS_316 VSS_317 VSS_318 VSS_319 VSS_320 VSS_321 VSS_322 VSS_323 VSS_324 VSS_325 VSS_326 VSS_327 VSS_328 VSS_329 VSS_330 VSS_331 VSS_332 VSS_333 VSS_334 VSS_335 VSS_336 VSS_337 VSS_338 VSS_339 VSS_340 VSS_341 VSS_342 VSS_344 VSS_345 VSS_346 VSS_347 VSS_348 VSS_349 VSS_350 VSS_351 VSS_352 VSS_353 VSS_354 VSS_355 VSS_356 VSS_357 VSS_358 VSS_359 VSS_360 VSS_361 VSS_362 VSS_363 VSS_364 VSS_365 VSS_366 VSS_367 VSS_368
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ED58 ED6 ED60 ED8 EE16 EE43 EE51 EF13 EF8 EH13 EH8 EK21 EK26 EK36 EK43 EK51 EK56 EK58 EL13 EL4 EL6 EL8 EN13 EN8 EP14 ER1 ER13 ER21 ER28 ER3 ER36 ER43 ER51 ER61 ER8 EU11 EU56 EU58 EU8 EV14 EV20 EV26 EV33 EV39 EV4 EV45 EV52 EV59 EW61 EY14 EY20 EY26 EY3 EY33 EY39 EY4 EY45 EY52 EY56 EY58 EY59 EY6 EY9 F21 F23 F26 F28 F30 F33 F4 F40 F46 F47 F52
@ ADL-P_BGA1744
UC1S
REV0.6
F56 F59 F9 FA40 FA7 FB1 FB14 FB26 FB42 FB48 FB59 FB61 FC2 FC55 FC56 FC58 FC60 G21 G25 G28 G31 G34 G42 G43 G50 H1 H13 H16 H18 H34 H37 H52 H58 H6 H8 H9 J11 J14 J17 J20 J21 J25 J28 J31 J36 J39 J47 J48 J51 J55 K4 L12 L13 L15 L17 L18 L20 L22 L23 L27 L30 L33 L35 L36 L38 L40 L54 L9 M16 M21 M26 M31 M32 M34
VSS_443 VSS_444 VSS_445 VSS_446 VSS_447 VSS_448 VSS_449 VSS_450 VSS_451 VSS_452 VSS_453 VSS_454 VSS_455 VSS_456 VSS_457 VSS_458 VSS_459 VSS_460 VSS_461 VSS_462 VSS_463 VSS_464 VSS_465 VSS_466 VSS_467 VSS_468 VSS_469 VSS_470 VSS_471 VSS_472 VSS_473 VSS_474 VSS_475 VSS_476 VSS_477 VSS_478 VSS_479 VSS_480 VSS_481 VSS_482 VSS_483 VSS_484 VSS_485 VSS_486 VSS_487 VSS_488 VSS_489 VSS_490 VSS_491 VSS_492 VSS_493 VSS_494 VSS_495 VSS_496 VSS_497 VSS_498 VSS_499 VSS_500 VSS_501 VSS_502 VSS_503 VSS_504 VSS_505 VSS_506 VSS_507 VSS_508 VSS_509 VSS_510 VSS_511 VSS_512 VSS_513 VSS_514 VSS_515 VSS_516
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M36 M47 M57 M59 N1 N4 N40 N41 N48 N54 N9 P11 P16 P21 P26 P3 P31 P35 P47 P51 P55 R12 R17 R22 R27 R32 R37 R44 R48 R58 T1 T11 T16 T21 T26 T3 T31 T35 T40 T52 U16 U21 U26 U31 U35 U44 U46 V3 V40 V41 V51 V55 V58 W1 W11 W16 W21 W26 W31 W35 W44 Y12 Y17 Y22 Y27 Y32 Y37 Y4 Y45 Y47 Y49 Y54
@ ADL-P_BGA1744
UC1P
REV0.6
A3 A10 A21 A23 A25 A26 A28 A30 A31 A33 A40 A47 A53 A60 AA11 AA21 AA26 AA31 AA35 AA40 AA44 AA57 AA59 AB16 AB21 AB26 AB31 AB35 AB54 AC4 AC40 AC44 AC51 AC55 AC6 AC8 AD21 AD26 AD31 AD35 AD46 AD48 AD58 AE12 AE17 AE22 AE27 AE32 AE37 AE40 AE44 AE52 AE9 AF4 AF46 AG1 AG51 AG55 AG58 AH9 AJ3 AJ41 AJ47 AJ49 AJ54 AK20 AK25 AK30 AK37 AK4 AK57 AK59 AK9
VSS_7 VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59 VSS_60 VSS_61 VSS_62 VSS_63 VSS_64 VSS_65 VSS_66 VSS_67 VSS_68 VSS_69 VSS_70 VSS_71 VSS_72 VSS_73
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AL15 AL17 AL22 AL4 AL41 AL54 AM11 AM3 AM51 AM55 AM9 AN17 AN40 AN46 AN48 AN58 AP1 AP15 AP20 AP22 AP25 AP35 AP51 AP55 AP9 AR4 AR54 AT47 AT57 AT59 AT6 AT8 AU54 AV11 AV4 AV9 AW1 AW14 AW51 AW55 AY1 AY43 AY46 AY48 AY51 AY55 AY58 AY9 B34 B4 B43 B50 B58 B61 BA4 BB12 BB54 BB6 BB8 BB9 BC14 BC47 BC57 BC59 BD4 BD54 BE1 BE12 BE51 BE55 BE9 BF46 BF48
@ ADL-P_BGA1744
UC1Q
REV0.6
BF58 BG1 BG12 BG44 BG52 BG9 BH4 BH46 BH48 BH58 BJ51 BJ55 BJ6 BJ8 BJ9 BL11 BL4 BL54 BL9 BM1 BM14 BM47 BM57 BM59 BN1 BN54 BN9 BP4 BP51 BP55 BR43 BR46 BR48 BR58 BR6 BR8 BR9 BT4 BT51 BT55 BU54 BU9 BV1 BV47 BV57 BV59 BW4 BW54 BW9 BY3 C1 C21 C25 C28 C31 C34 C40 C47 C9 CA14 CA43 CA46 CA48 CA51 CA55 CA58 CB4 CB6 CB8 CB9 CC1 CC52 CD46
VSS_149 VSS_150 VSS_151 VSS_152 VSS_153 VSS_154 VSS_155 VSS_156 VSS_157 VSS_158 VSS_159 VSS_160 VSS_161 VSS_162 VSS_163 VSS_164 VSS_165 VSS_166 VSS_167 VSS_168 VSS_169 VSS_170 VSS_171 VSS_172 VSS_173 VSS_174 VSS_175 VSS_176 VSS_177 VSS_178 VSS_179 VSS_180 VSS_181 VSS_182 VSS_183 VSS_184 VSS_185 VSS_186 VSS_187 VSS_188 VSS_189 VSS_190 VSS_191 VSS_192 VSS_193 VSS_194 VSS_195 VSS_196 VSS_197 VSS_198 VSS_199 VSS_200 VSS_201 VSS_202 VSS_203 VSS_204 VSS_205 VSS_206 VSS_207 VSS_208 VSS_209 VSS_210 VSS_211 VSS_212 VSS_213 VSS_214 VSS_215 VSS_216 VSS_217 VSS_218 VSS_219 VSS_220 VSS_221
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CD58 CE51 CE55 CF47 CF49 CF54 CG57 CG59 CH11 CH12 CH54 CH6 CH8 CH9 CJ14 CJ4 CJ44 CK1 CK3 CK43 CK46 CK48 CK51 CK55 CK58 CM52 CN46 CN58 CP51 CP55 CR43 CR47 CR49 CR54 CT11 CT57 CT59 CT6 CT8 CT9 CU4 CU54 CV14 CW43 CW46 CW48 CW51 CW55 CW58 CY51 CY55 D11 D14 D17 D20 D21 D25 D28 D31 D4 D53 D56 D58 D59 D9 DA11 DA12 DA6 DA8 DA9 DB14 DB4 DB54
@ ADL-P_BGA1744

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Issued Date	2020/10/15	Deciphered Date	2021/04/15

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Title: **P017 - ADL-P(12/13)GND**

Size: | Document Number: **LA-L652P** | Rev: 1.0(A00)

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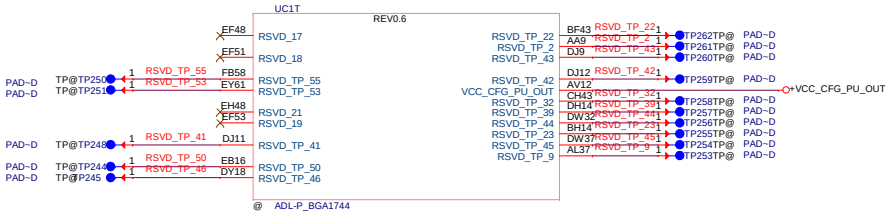

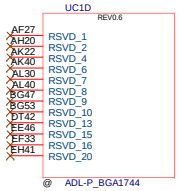

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Title: **P018 - ADL-P(13/13)RSVD**

Size: | Document Number: **LA-L652P** | Rev: 1.0(A00)

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Title: **P019 - Reserve**

Size	Document Number	Rev
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Title: **P020 - Reserve**

Size	Document Number	Rev
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Issued Date	2020/10/01	Deciphered Date	2021/04/15

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Compal Electronics, Inc.

Title: **P021 - Reserve**

Size	Document Number	Rev
	LA-L652P	1.0(A00)

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Main Function:

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Title: RSV			
Size	Document Number: LA-L652P		Rev: 1.0(400)
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STD type connector

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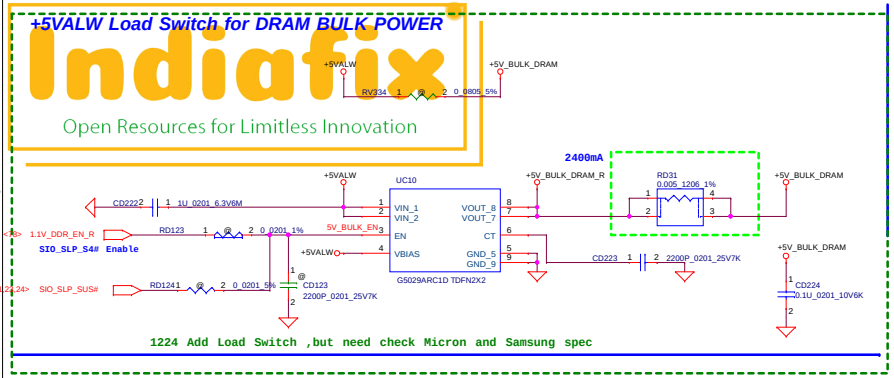
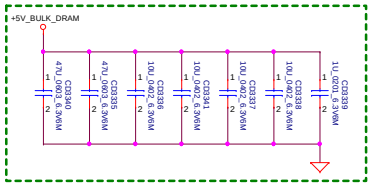
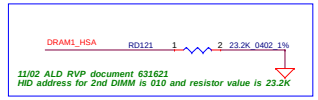
+5VALW Load Switch for DRAM BULK POWER



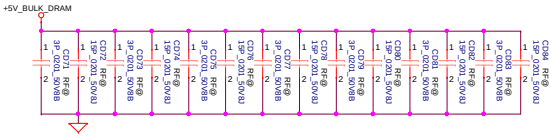
1224 Add Load Switch ,but need check Micron and Samsung spec



1104 DDR5 SODIMM request ,+5V_BULK_DRAM cap.



11/02 ALD RVP document 631621
HID address for 2nd DIMM is 010 and resistor value is 23.2K

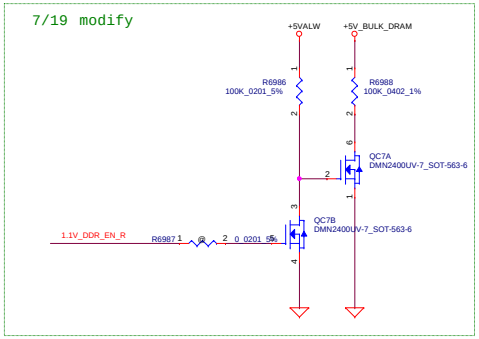


1110 Del no use Cap

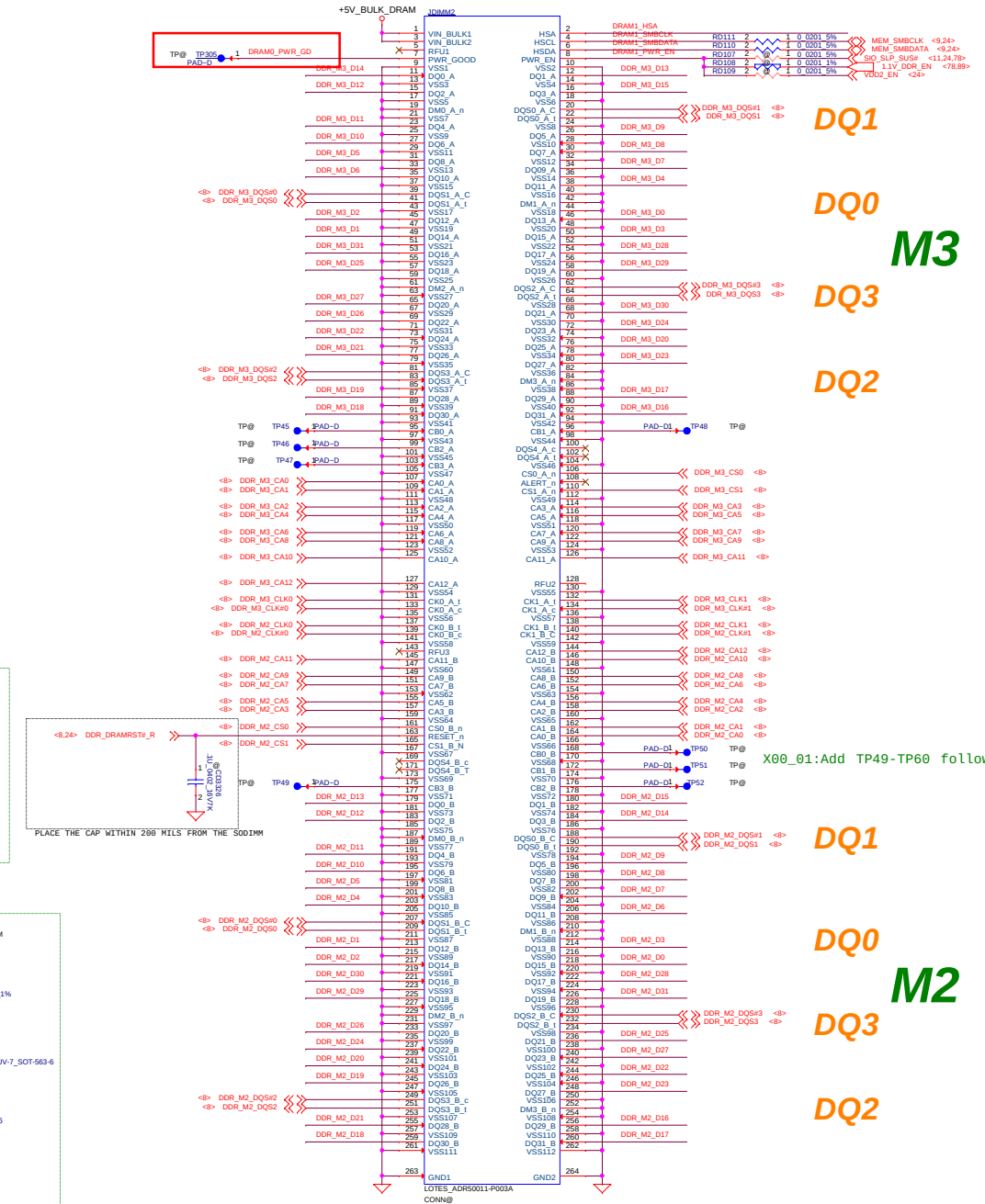
1103 Del SODIMM DDR4 Chanel strap pin
Del SA0,SA1,SA2

X00_01:Add TP49-TP60 follow RVP

7/19 modify



1103 Del SODIMM DDR4 Vref pin
DDR5 VREF doesn't to connect to CPU



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.	
Title	P023 - DDR4 DIMMA
Size	Document Number: LA-L652P Rev: 1.0(400)
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Layout Note:
Place near JDIMM2.257,259

Reverse type connector

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<8> DDR_M0_D[0..31]
<8> DDR_M1_D[0..31]

+5V_BULK_DRAM

close to CD3348

ESD@ DT25 TVNST2302AB0_SOT-523-3 SCA000001W00

1104 DDR5 SODIMM request ,+5V_BULK_DRAM cap.

+5V_BULK_DRAM

DRAM0_HSA RD122 1 2 10K_0402_1%

11/02 ALD RVP document 631621
HID address for 1st DIMM is 000 and resistor value is 10K

1110 Del no use Cap

1103 Del SODIMM DDR4 Chanel strap pin
Del SA0,SA1,SA2

1103 Del SODIMM DDR4 Vref pin
DDR5 VREF doesn't to connect to CPU

<8,23> DDR_DRAMRST#_R

PLACE THE CAP WITHIN 200 MILS FROM THE SODIMM

+5V_BULK_DRAM

JDIMM1

TP@ TP306 PAD-D DRAM1_PWR_GD

1026 Modify DDR foorprint and Data/CLK pin define

DQ3 DQ2 M1 DQ1 DQ0

X00_01:Add TP49-TP60 follow RVP

DQ1 DQ0 M0 DQ3 DQ2

LOTES_ADR50012-P003A
LOTES_ADR50012-P003A
CONN@

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Issued Date	2019/11/30	Deciphered Date	2021/04/15

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Compal Electronics, Inc.

Title: P024 - DDR4 DIMMB

Size: | Document Number: LA-L652P | Rev: 1.0(400)

Date: Wednesday, December 15, 2021 | Sheet 24 of 120

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VRAM X76:

8G bit GDDR6					
New Hynix 4GB SKU		Samsung 4GB SKU		Hynix 4GB SKU	
R1	R3	R1	R3	R1	R3
UM0 VNHBGR3@ MT61K256M32JE-14:A1.2V SA0000ENPZL RG80 VNH@ 100K +-5% 0201 SD043100380 UM10 VNHBGR3@ MT61K256M32JE-14:A1.2V SA0000ENPZL RG83 VNH@ 100K +-5% 0201 SD043100380 UM11 VNHBGR3@ MT61K256M32JE-14:A1.2V SA0000ENPZL RG84 VNH@ 100K +-5% 0201 SD043100380 UM12 VNHBGR3@ MT61K256M32JE-14:A1.2V SA0000ENPZL		UM0 VS8GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L RG81 VS@ 100K +-5% 0201 SD043100380 UM10 VS8GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L RG83 VS@ 100K +-5% 0201 SD043100380 UM11 VS8GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L RG85 VS@ 100K +-5% 0201 SD043100380 UM12 VS8GR3@ K4ZB0325BC-HC14 1.2V SA0000C626L		UM9 VH8GR1@ H56C8H24AIR-S2C SA0000DUW1L RG81 VH@ 100K +-5% 0201 SD043100380 UM10 VH8GR1@ H56C8H24AIR-S2C SA0000DUW1L RG82 VH@ 100K +-5% 0201 SD043100380 UM11 VH8GR1@ H56C8H24AIR-S2C SA0000DUW1L RG85 VH@ 100K +-5% 0201 SD043100380 UM12 VH8GR1@ H56C8H24AIR-S2C SA0000DUW1L

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GC OFF 1.0 GPU Power ON/OFF

DVT2 need to edit BOM config

PEX_WAKE# doesn't apply in notebook MBD

Under GPU

Near GPU

16 mils

Place this pull down resistor as close as possible to GPU

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Issued Date	2018/08/07	Deciphered Date 2021/04/15	Title: NV(1/8) PCI EXPRESS
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			Date: Wednesday, December 15, 2021; Sheet 28 of 120

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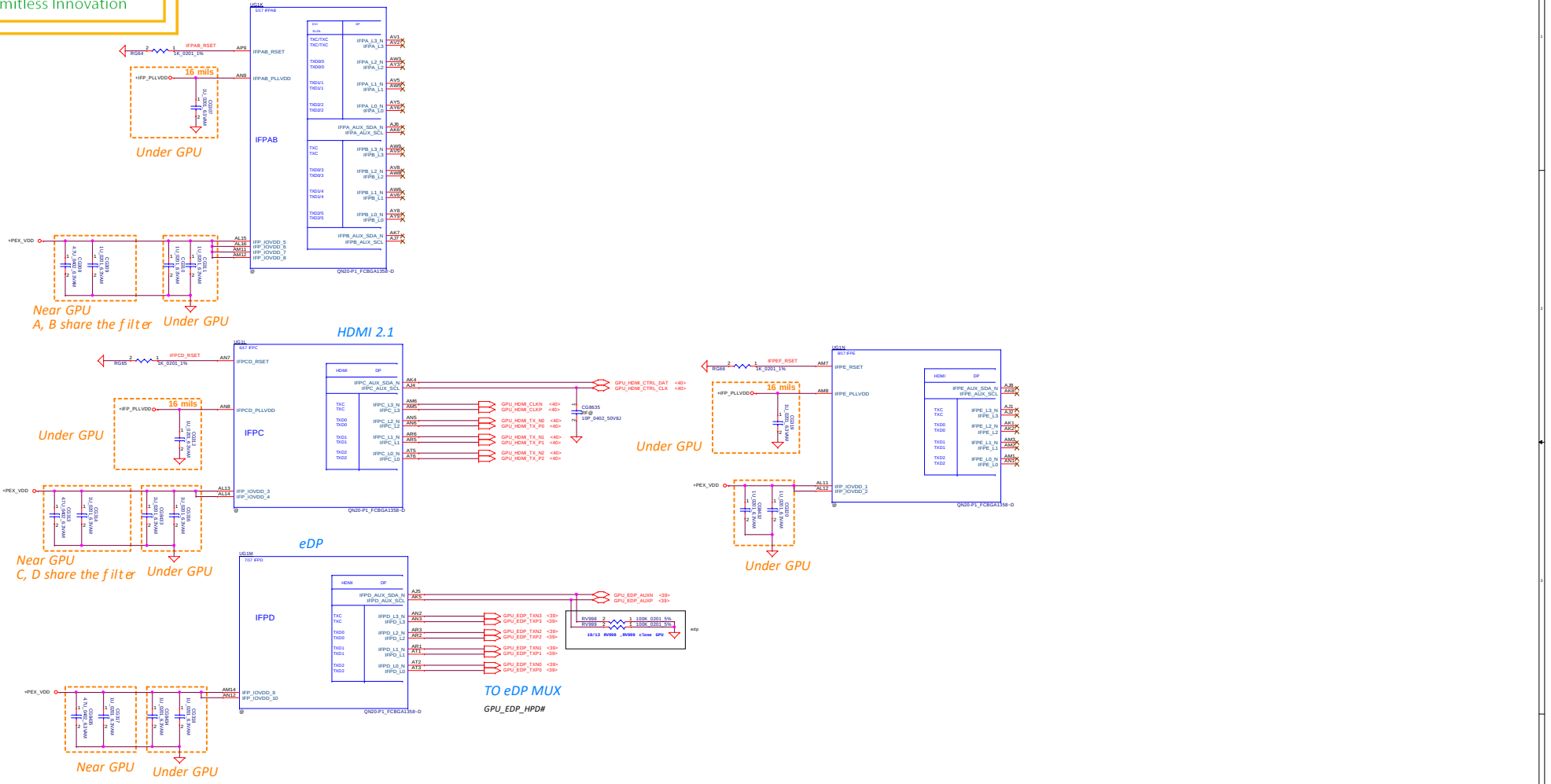

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			Size: Document Number: LA-L652P Rev: 1.0(0.0)
			Date: Wednesday, December 15, 2021 Sheet 27 of 120

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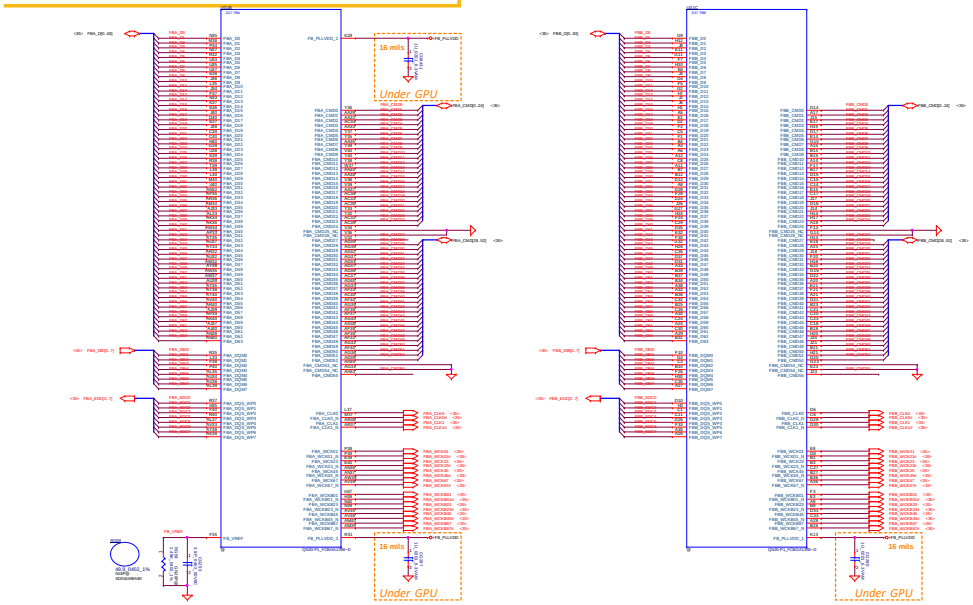

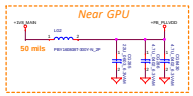

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			Title: NV93(8) MEMORY_FB_ABCD
			Size: LA-L652P
			Date: Document Number: Rev: 1.0A
			Sheet 38 of 48

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External current sense for power monitoring

By 5/6 modify

GPU To PWR PSI

7/29 EVT modify

connection to POWER

For N18P 1V8_MAIN EN to NVDD_EN RC delay

E board

9/7 DVT1 modify
Remove RX48 (0 ohm)

9/7 DVT1 modify
Change to +1V8_AON

Security Classification	Compal Secret Data	
Issued Date	2018/08/07	Deciphered Date 2021/04/15

Compal Electronics, Inc.

Title: NV(4/8) GPIO

Size: Document Number: LA-L652P

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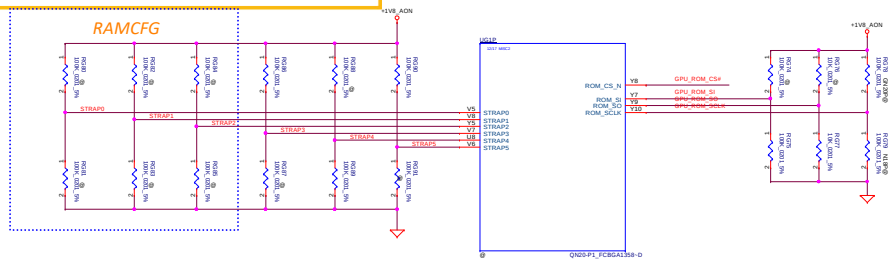
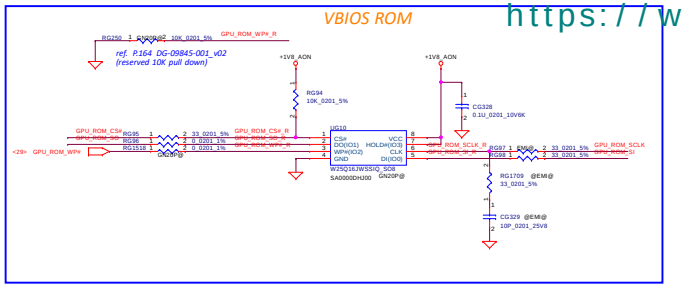
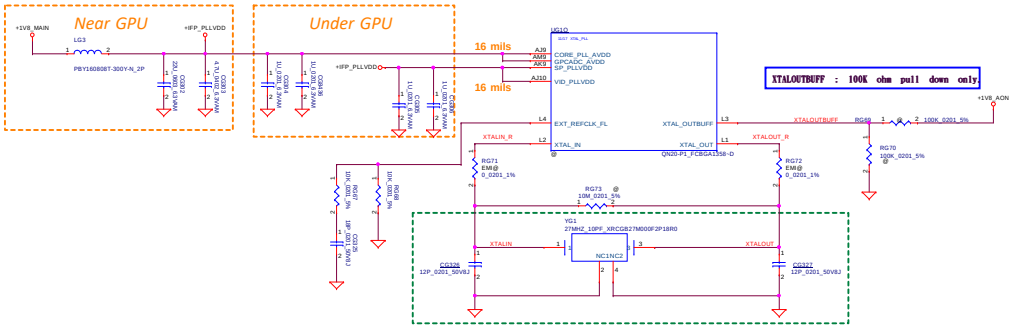
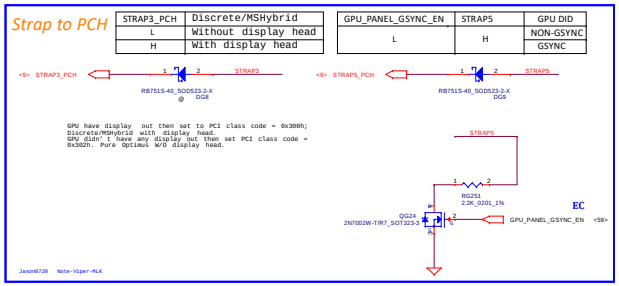
GDDR6 VRAM	Strap0	Strap1	Strap2
SAMSUNG	L	L	L
HYNIX	L	H	L
New HYNIX	H	L	H









STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

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Issued Date	2020/03/05	Deciphered Date	2021/04/15
			Title: NV(4/8) STRAP, ROM, XTAL
			Size: D; Document Number: LA-L652P; Rev: 1.0(0.0)
			Date: Wednesday, December 15, 2021; Sheet 30 of 120

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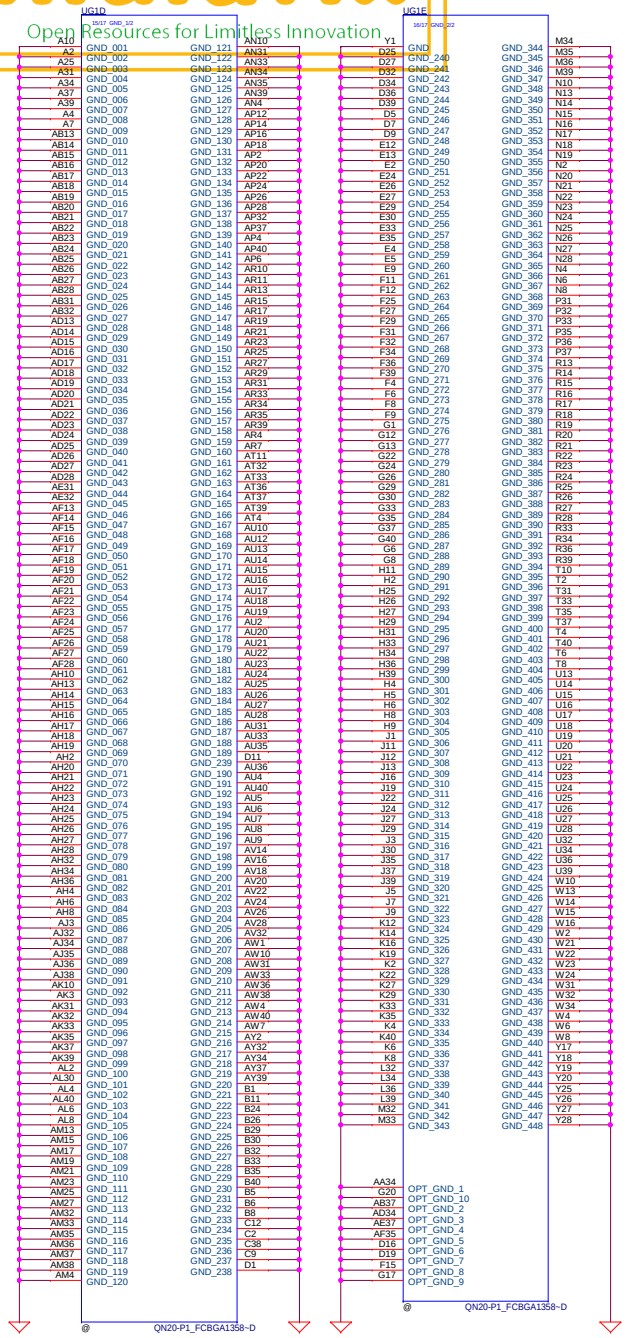

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Title: **NV(6/8) GND, RFUs**

Size	Document Number	Rev
	LA-L652P	1.0(A00)

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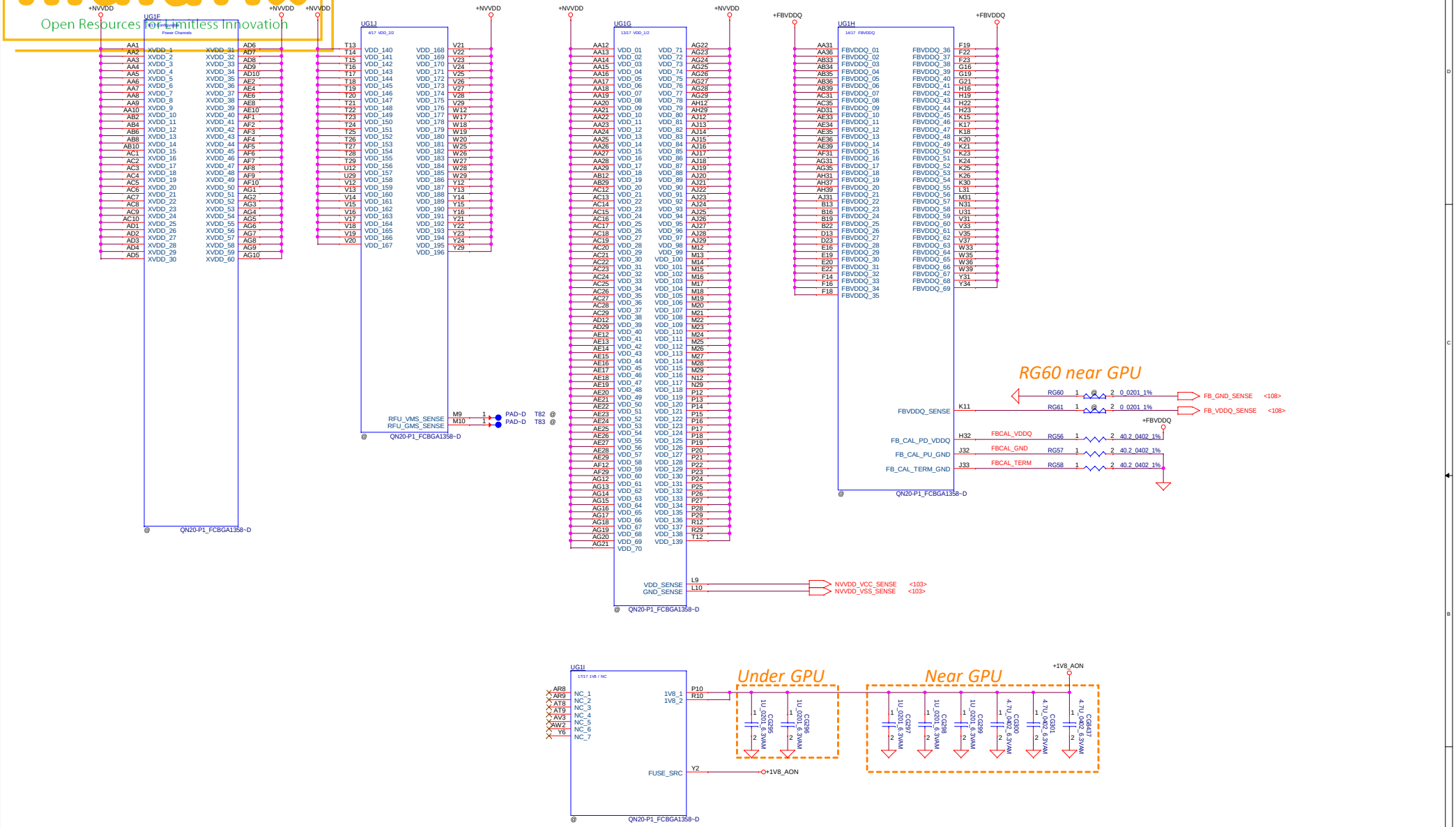

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Compal Electronics, Inc.

Title: NV(7/8) POWERS

Size	Document Number	Rev
	LA-L652P	1.0(A00)

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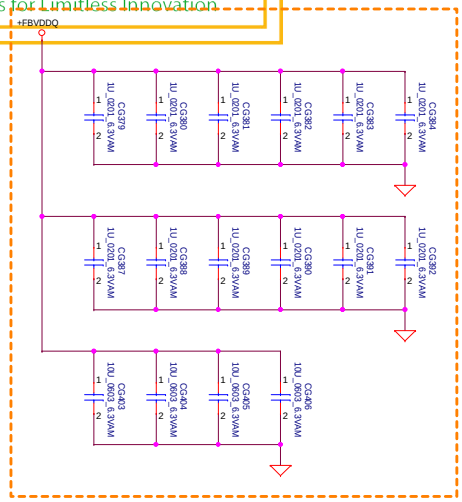
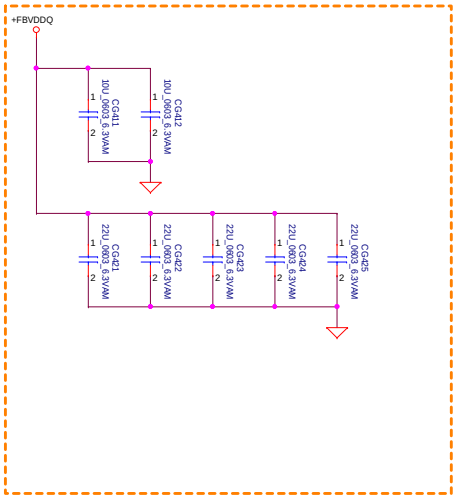
FBVDDQ_GPU

Under GPU



Near GPU



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Compal Electronics, Inc.

Title: **NV(8/8) GPU DECOUPLING**

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OVRM Gen1 with N18P-G61-A

OVRM Gen2 with GN20P0/P1

SA0000CQX00

SH_O BOM option

SH_IN BOM option

BS_REF BOM option

BS_IN BOM option

other

11/06 DVT1 change to 0402 package
11/13 Change to 10ohm and stuff for GC6 Sequence

11/06 DVT1 change to 0402 package

7/24 Reserve

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Compal Electronics, Inc.

Title: OC, Discharging

Size: | Document Number: LA-L652P | Rev: 1.0(00)

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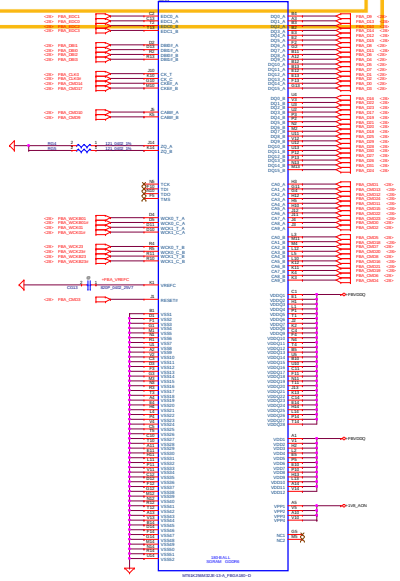
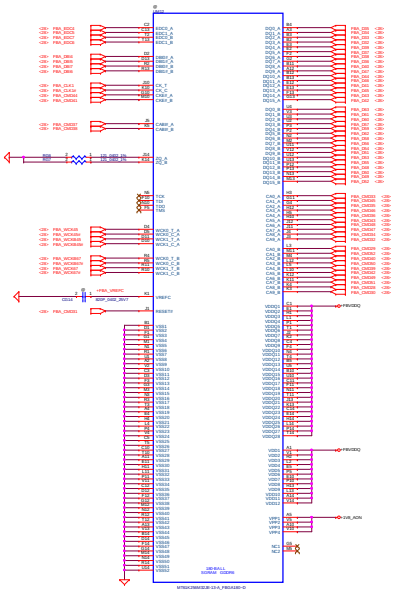
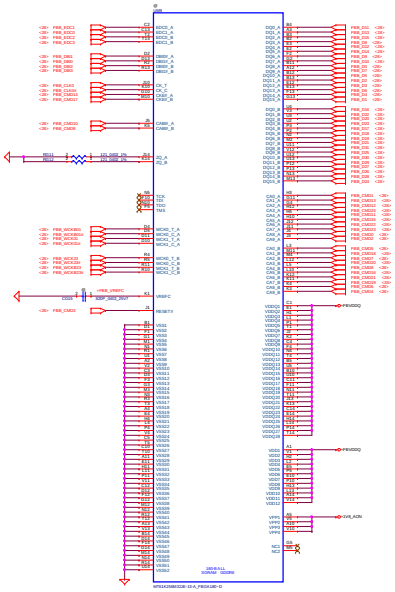
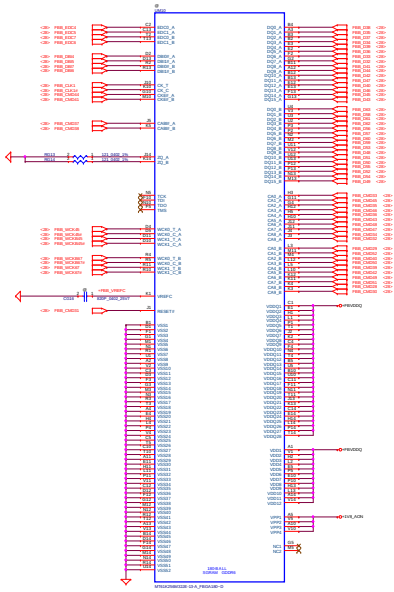
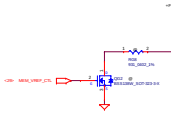
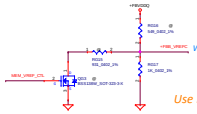




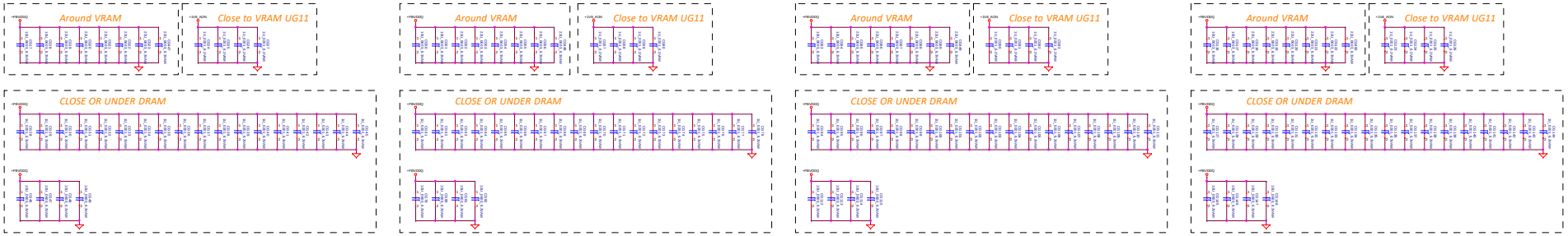








UM11 UM12 UM9 UM10



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			VRAM_GDDR6_AB
			LA-L652P

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Title

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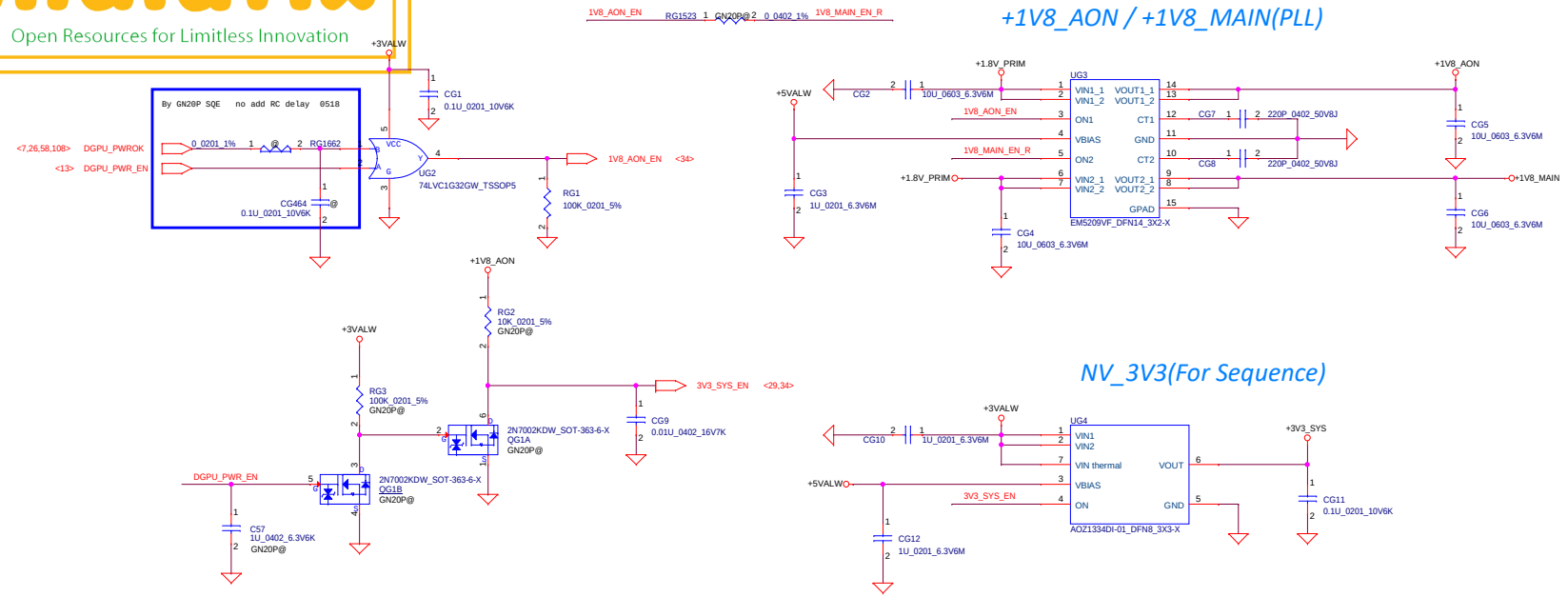
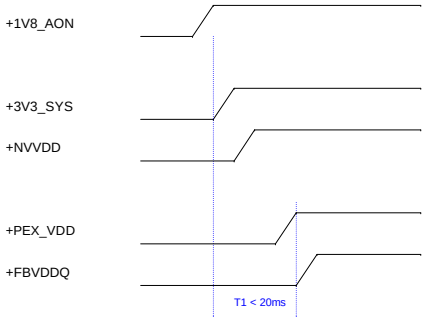
+1V8_AON / +1V8_MAIN(PLL)



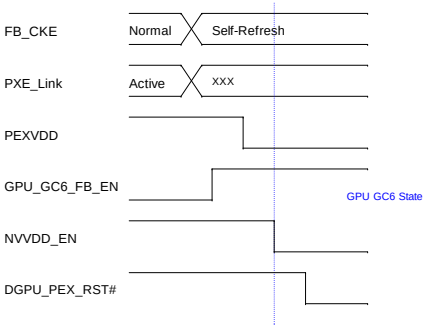
NV_3V3(For Sequence)

GPU Power Up Sequence



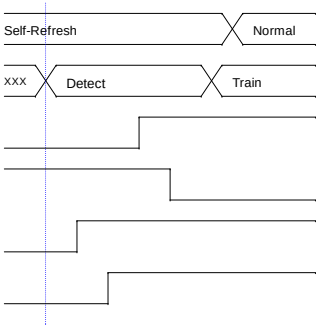
The ramp time for any rail must be more than 40us and less than 2ms.

GPU GC6 Entry Sequence

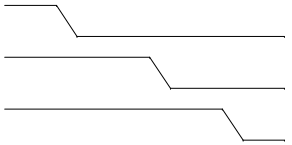


The entire entry/exit sequence must complete within 200 ms.

GPU GC6 Exit Sequence



GPU Power Down Sequence



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Compal Electronics, Inc.

Title: **DGPU_DC/DC Interface**

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Main Func = LCD

CPU
GPU
BL_EN
DDS
EC-DDS
EC-BKOFF
Backlight
EC (BIST MODE)
9/15 DVT2 change to two diode

Refer PS8461E design, change 0.1u to 0.22u

No AUX Cap in PS8461E vendor's reference design (6/19)

Pin 30 RSV for NV/non-NV

W=60 mils

1.5A

Need connect to EC

Main Func = DMIC

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From Module

10/22 DVT1 change to 0ohm

DMIC 3V POWER

DMIC 3.3V POWER

To CPU

DATA OUTPUT

From Module

DATA INPUT

modify by 9/7 because layout

Main Func = LCDVDD monitor

For BL_PWR_SRC & LCDVDD monitor

place as close as QV4

Main Func = Hinge up protection

use SA0000E0700 (G2895BLK21U)

EC (BIST MODE)

LCD_EN

3/8 Add

PCH

GPU

Non-DDS

DDS

9/15 DVT2 change to two diode

EC-DDS
Panel RST

3/8 Add

EC

High Active

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Compal Electronics, Inc.

Title: eDP/Camera

Size: Document Number: LA-I652P Rev: 1.0(A00)

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Main Func = eDP DDS PWM

9/12 DVT1 modify
Change DDS detect logic to "Low" (EC)

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PU on EC side

To PWM Switch

To MUX Switch

BL_PWM

9/12 DVT1 modify

PU on EC side

EN#	IN	NC to COM COM to NC	NO to COM COM to NO	Function
L	L	ON	OFF	IGPU
L	H	OFF	ON	DGPU
H	X	OFF	OFF	X

9/16 DVT1 modify
For 360Hz Panel support (Min PWM level 3.0)

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Main Func = eDP DDS MUX

PS8461=3.3V , 210 mA

Refer PS8461E design

UV20 need modify symbol

GPU Side

CPU Side

eDP

Refer PS8461E reference design 9/2

Refer PS8461E design

EQ Value

need the bom suggestions from vendor

MUX Switch	EDP_SW
0(Default)	IGPU
1	DGPU

+1.2V_RUN power ripple need <30mV

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Compal Electronics, Inc.

Title: eDP MUX/DDS

Size: Document Number: LA-L652P Rev: 1.0(0.0)

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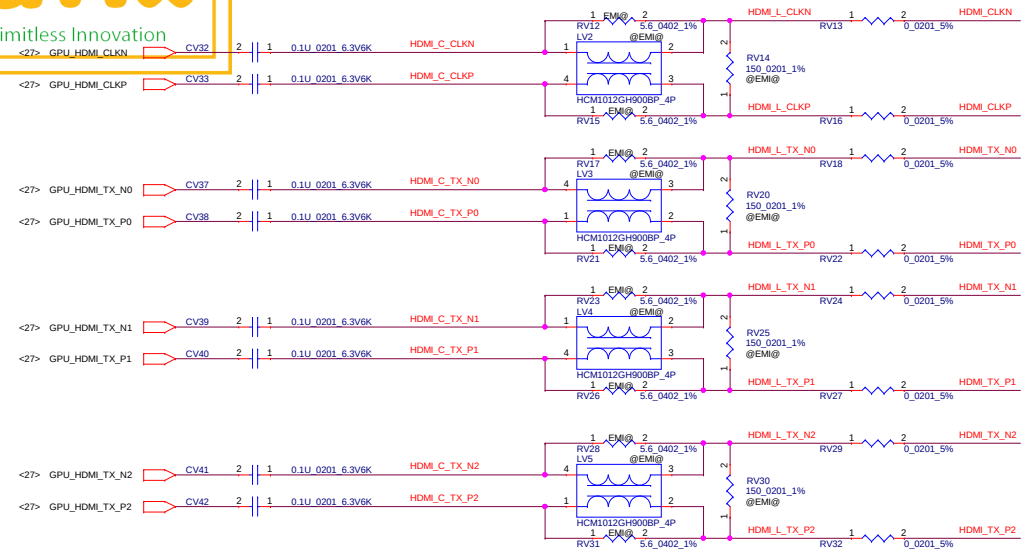

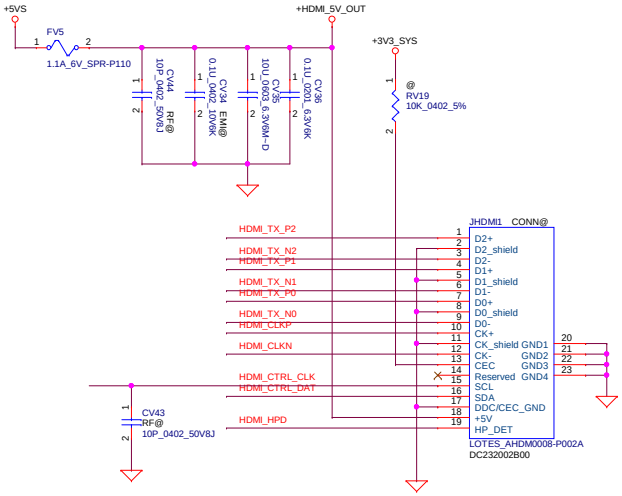

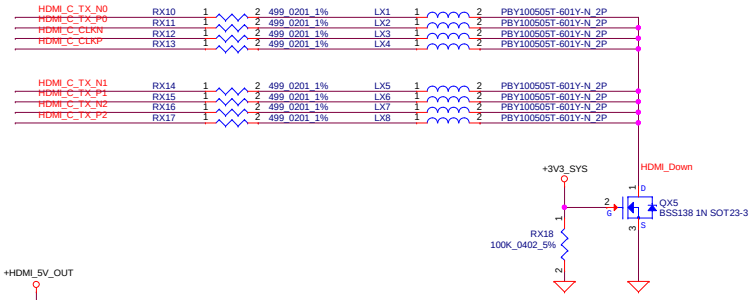

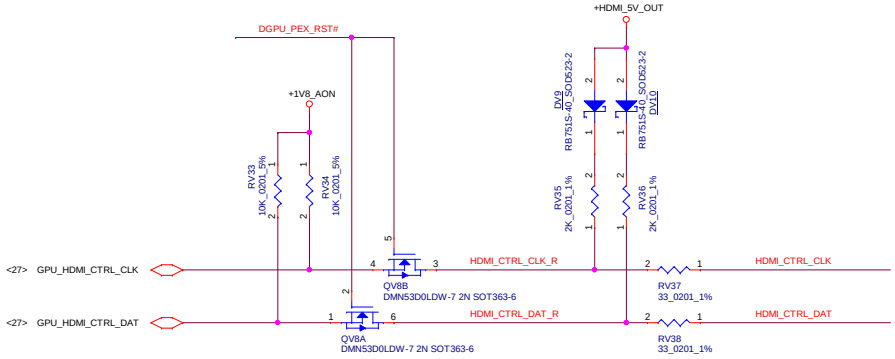

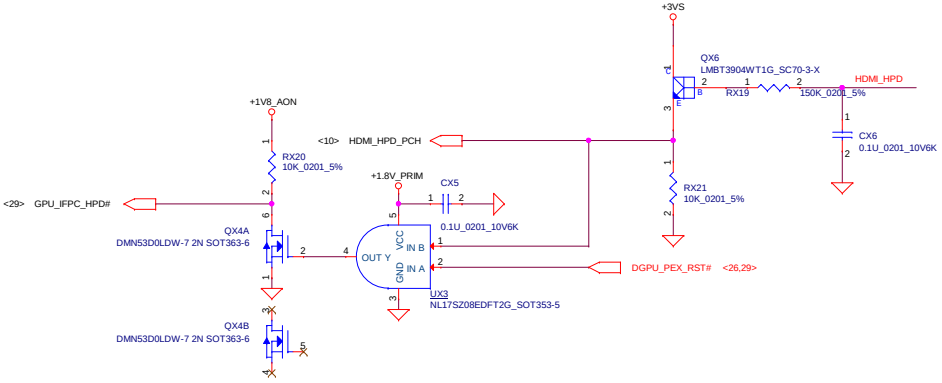

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Title: **HDMI**

Size	Document Number	Rev
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Reserve

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Compal Electronics, Inc.			
Title: RSV			
Size	Document Number: LA-L652P		Rev: 1.0(400)
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Title	RSV	
Size	Document Number	Rev
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Compal Electronics, Inc.		
Title: Thunderbolt (2/2)		
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+3VALW_R_PD

+5VALW_R_PD

+TBT_VBUS_R

+VCC3V3_PD_LDO

2.2K_0201_5% RPD209 I2C3_PD_R_CLK_R
2.2K_0201_5% RPD210 I2C3_PD_R_DAT_R
10K_0201_5% RPD184 PD_PROCHOT#
10K_0201_5% RPD137 PD_R_USB_MUX_FLIP#

+3VALW_R_PD

2.2K_0201_5% RT80 UPD1_SMBCLK
2.2K_0201_5% RT149 UPD1_SMBDAT
10K_0201_5% RT78 UPD1_SMBINT#

100K_0201_5% RPD225 PD_R_EN_HV_1_R
100K_0201_5% RPD136 PD_R_USB_MUX_FLIP#

need change PN to SA0000EEE00

UPD1 SN20100019RSMR SA0000EEE00

+VCC1V5_PD_LDO CPD16 10U_0402_10V6M
+VCC3V3_PD_LDO 3V/25 mA CPD14 10U_0402_10V6M

VIN_3V3, VBUS_1, VBUS_2, PP5V_1, PP5V_2, LDO_3V3, LDO_1V5

GPIO0, GPIO1/HPD_TX, GPIO2, GPIO3/HPD_Rx, GPIO4/USB_P, GPIO5/USB_N, GPIO6, GPIO7, GATE_VBUS, GATE_VSYS, VSYS, ADCIN1, ADCIN2, CC1, CC2, GND, THERMAL_PAD

PD_PROCHOT#, PD_R_USB_MUX_FLIP#, PD_R_USB_MUX_EN, PD_R_EN_HV_1_R

TP174 TP@ PAD-D
TP173 TP@ PAD-D

CPD388 330P_0402_50V7K
RPD290 0_0201_1%
ADCIN1_R_PD
ADCIN2_R_PD
TBT_CC1_R, TBT_CC2_R
RT653, RT654 0_0201_5%
TBT_CC1 <45>, TBT_CC2 <45>
CPD12, CPD13 330P_0201_50V7K

SN1905023RSMR_QFN32_4X4-X

By 5/7 modify

RPD186 0_0201_1% TCP0_HPD <6>, PROCHOT# <7,18>
RPD135 0_0201_1% GPIO5 PD_USB_MUX_FLIP# <45>
RPD221 0_0201_1% PD_USB_MUX_EN <45>

I2C1(Slave) from EC

<58> UPD1_SMBCLK, <58> UPD1_SMBDAT, <58> UPD1_SMBINT#
RPD165, RPD166, RPD109 0_0201_5%
I2C1_PD_R_CLK, I2C1_PD_R_DAT, I2C1_PD_R_INT#
I2C_EC_SCL, I2C_EC_SDA, I2C_EC_IRQ **EC**

I2C2(Slave) from CPU

<9> SML1_SMBCLK, <9> SML1_SMBDATA, <11> I2C2_PD_INT#
RPD105, RPD106, RPD113 0_0201_5%
I2C2_PD_R_CLK, I2C2_PD_R_DAT, I2C2_PD_R_INT#
I2C2s_SCL, I2C2s_SDA, I2C2s_IRQ **CPU**

I2C3_PD_R_CLK_R, I2C3_PD_R_DAT_R
I2C3m_SCL, I2C3m_SDA, I2C3m_IRQ

Right PD Controller SPI FLASH

+VCC3V3_PD_LDO
I2C3_PD_R_CLK_R, I2C3_PD_R_DAT_R
PD_R_A0, PD_R_A1, PD_R_A2
UPD4 CAT24C256HU4IGT3_UDFN8_2X3 (SCL, SDA, VCC, A0, A1, A2, VSS, GND, WP)
RPD217 10K_0201_5%, RPD218 10K_0201_5%
CPD11 0.1U_0201_10V6K
RPD216 10K_0201_5%

PD SPI ROM Remove in MP

EVT_25

+VCC3V3_PD_LDO
RPD289 10K_0201_5%
GPIO5 RPD192 0_0201_1%

I2C3_PD_R_DAT, I2C3_PD_R_CLK
I2C1_PD_R_CLK, I2C2_PD_R_CLK, I2C2_PD_R_DAT, I2C2_PD_R_INT#, I2C1_PD_R_DAT, I2C1_PD_R_INT#
JCCG1
GND1, GND2
ACES_50521-01041-P01
DBCONN@

DIV = R2/(R1+R2)
ADCIN1 = 2 (0.09)
ADCIN2 = 0
Port R Address: 0x22

+VCC3V3_PD_LDO
R1 RPD102 100K_0201_1% ADCIN1_R_PD
R2 RPD101 10K_0201_1%
+VCC3V3_PD_LDO
R1 RPD99 100K_0201_1% ADCIN2_R_PD
R2 RPD89 10K_0201_1%

GPIO	Pin #	Package Pin Name	TPS65992D		
			TGL w/ Burnside Bridge RT	RKL w/o TBT	RKL w/ TR or MR
0	5	GPIO0	-	-	-
1	6	GPIO1 (HPD_Tx)	RT_EN	HPD_Tx	-
2	7	GPIO2 (PROCHOT#)	PROCHOT#	PROCHOT#	PROCHOT#
3	19	GPIO3	RT_RST	-	TBT_RST
4	26	GPIO4 (USB_P)	DDM_MUX_FLIP*	DDM_MUX_FLIP*	DDM_MUX_FLIP*
5	27	GPIO5 (USB_N)	DDM_MUX_EN*	DDM_MUX_EN*	DDM_MUX_EN*
6	17	GPIO6	USB2_MUX_EN*	USB2_MUX_EN*	USB2_MUX_EN*
7	36	GPIO7	-	-	-

Table 2: Decoding of ADCIN1 and ADCIN2 pins.

DIV = R_{LOAD} / (R_{UP} + R_{LOAD})[1] MIN	MAX	Without using R_{UP} or R_{LOAD}	ADCINx decoded value
0	0.0928	tie to GND	0
0.1029	0.1272	N/A	1
0.1723	0.1425	N/A	2
0.1425	0.2372	N/A	3
0.2373	0.3671	N/A	4
0.3672	0.7064	tie to LDO_1V5	5
0.7065	0.9998	N/A	6
DIV = R_{LOAD} / (R_{UP} + R_{LOAD})[1] MIN	MAX	Without using R_{UP} or R_{LOAD}	ADCINx decoded value
0.9081	1.0	tie to LDO_3V3	7

Table 6. Device Configuration using ADCIN1 and ADCIN2 .

ADCIN1 decoded value [1]	ADCIN2 decoded value [1]	I²C address index [2]	Dead Battery Configuration
7	5	#1	AlwaysEnableSink. The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
2	0	#3	
1	7	#4	
7	4	#1	SinkRequires_3.0A. The device only enables the sink path if the attached source is offering at least 3.0A. USB PD is disabled until configuration is loaded.
4	4	#2	
3	0	#3	
2	7	#4	
7	6	#1	SinkRequires_1.5A. The device only enables the sink path if the attached source is offering at least 1.5A. USB PD is disabled until configuration is loaded.
6	6	#2	
6	5	#3	
6	7	#4	
7	3	#1	HaighAvailableVoltage [3]. The device always enables the sink path during the initial implicit contract regardless of the amount of current the attached source is offering. The PD controller will enter the "APS" mode, enable USB PD PHY and negotiate a contract for the highest power contract that is offered up to 20 V.
3	3	#2	
4	0	#3	
3	7	#4	
7	0	#1	SafeMode. The device does not enable the sink path. USB PD is disabled until configuration is loaded. Note that this configuration could put the device into a source-only mode.
0	0	#2	
6	0	#3	
5	7	#4	

Table 5. I²C Default Slave Address for I2C_EC_SCL/SDA.

I²C address index (decoded from ADCIN1 and ADCIN2)[1]	Port	Slave Address Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		Available During BOOT
#1	A	0	1	0	0	0	0	0	R/W		Yes
#2	A	0	1	0	0	0	0	1	R/W		Yes
#3	A	0	1	0	0	0	1	0	R/W		Yes
#4	A	0	1	0	0	0	1	1	R/W		Yes

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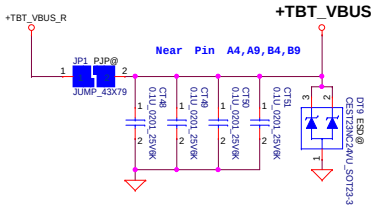
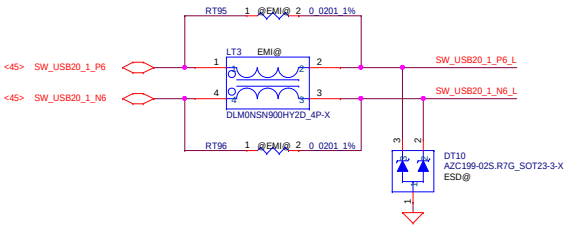
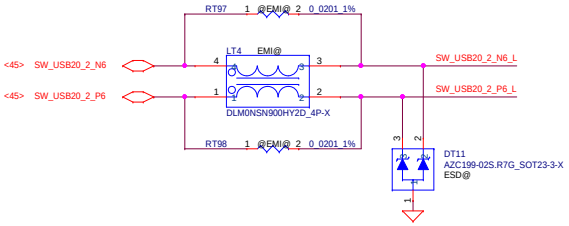
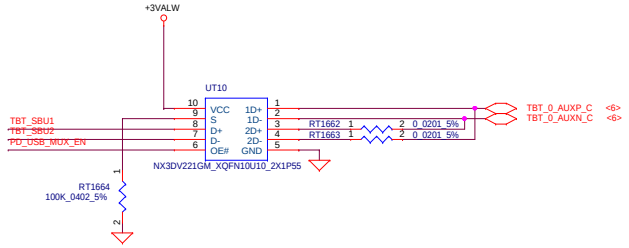
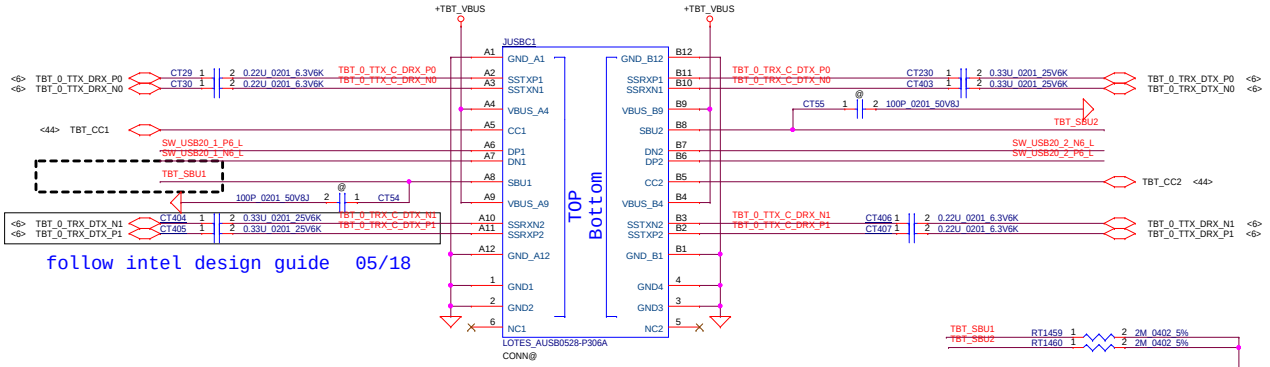


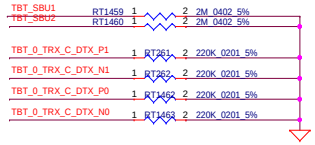






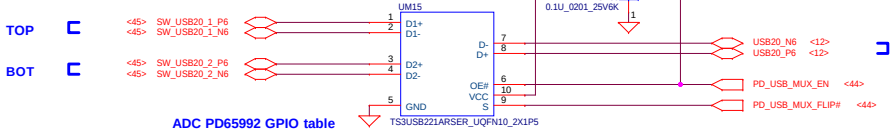


follow intel design guide 05/18

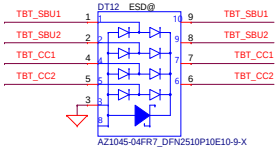


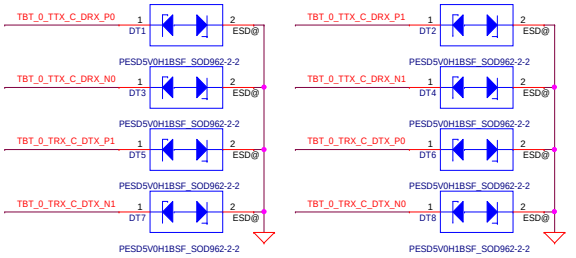
USB2 MUXES_R

Close JUSBC1



ADC PD65992 GPIO table





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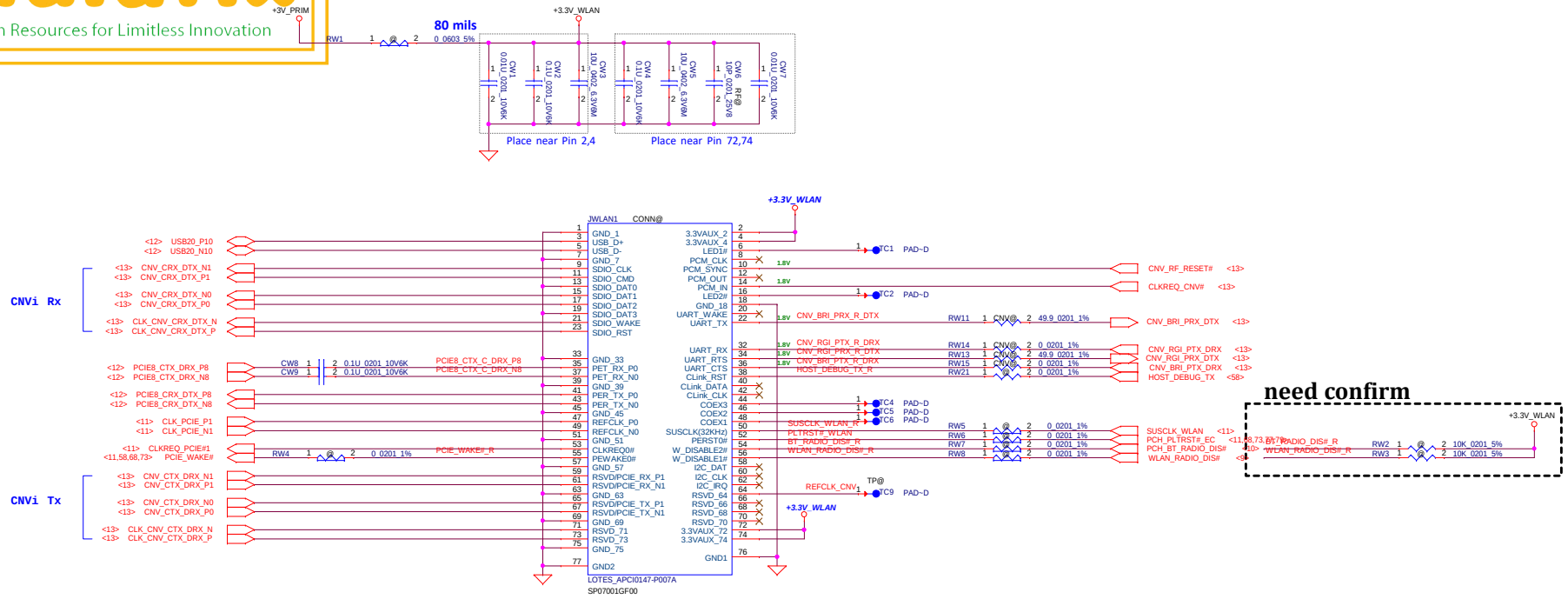

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+3VALW

CML+P no pull hgih

+3VALW_EC

+1.8V_PRIM

Every 0.1uF decoupling capacitor should close to designated UE1 power pin within 200 mil

modify by 0525

close to D1

+RTC_CELL

Model ID

Board ID

SD034274280

SD034174280

SD000009K00

SD034887280

MCU/GPU/SSD/Thermal
BATT/Charger
Touch Pad
TypeC PD/IO Expendor

modify by 0519

MCU/GPU/SSD/Thermal
BATT/Charger
Touch Pad
TypeC PD/IO Expendor

close to C1

from Hinge

BSS strap

Boot Source Select Strap
0=Use the Shared SPI Chan for Boot
1=Use the eSPI Flash Channel for Boot

SYSPWR_PRES

SHD_CS0#

CR strap

trace length should not exceed 250mil

modify by 0527

GPIO86 don't ph
prevent booter into UART update mode

RE31 close to E1

Close to UE1 pin A37

Close to UE1 pin A61

close to F3

close to F2

Intel chipset

GPO65 don't ph
prevent booter into UART update mode

32.768KHz Oscillator

SJ00000C100

modify by 0525

modify by 0715

ref. Fiorano MLK

Place QE6 closer CPU side
Place CE30 close to the QE16 as possible

TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO170	JTAG_STRAP	1=Use the JAG TAP Controller for Boundary Scan 0=The JTAG TAP Controller is used for debug (normal operation)	VTR1
GPIO104	VTR2_STRAP	Voltage Level strap is used to determine if the Shared Flash interface must be configured for 3.3V or 1.8V operation 1= 3.3V Operation 0= 1.8V Operation	VTR1
GPIO045	CR_STRAP	Crisis Recovery Strap 1=Normal Boot Source 0=Use the Private SPI pins to boot from Crisis Recovery flash over Keyscan connector Note: This pin requires an external pull-up for normal operation.	VTR1
GPIO207	CMP_STRAP	CMP_STRAP is the Comparator 0 Strap pin. This strap must be enabled in EFUSE 0=Hardware Default (GPIO input) 1=Comparator 0 Enabled	VTR1
GPIO055/SHD_CS 0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for Boot 0=Use the eSPI Flash Channel for Boot	VTR2
GPIO227/SHD_IO2	PWRGD_STRAP	Primary Power rails good 1 = Primary power rails are good 0 = Primary power rails not stable	VTR2

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Title: RSV

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Main Func = GPIO Expander

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Control Byte

0	1	0	0	A2	A1	A0	R/W

R/W = 0 = Write
R/W = 1 = Read
SMbus address 0x40

10/21 DVT1 modify from TP I2C to PD I2C

5/14 modify pin def i ne

5/23 add

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

WDT

S5 LID CLOSE

11/4 DVT1 modify for material preparat i on SC100000S00 change to SCS00006300

10/21 DVT1 Add

1006 DVT1 modify

place close to UE4.14.24

Add By 7/5 For IT8306 colay

11/4 DVT1 modify for material preparat i on SC100000S00 change to SCS00006300

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Title: GPIO Expander/WDT/S5 LID

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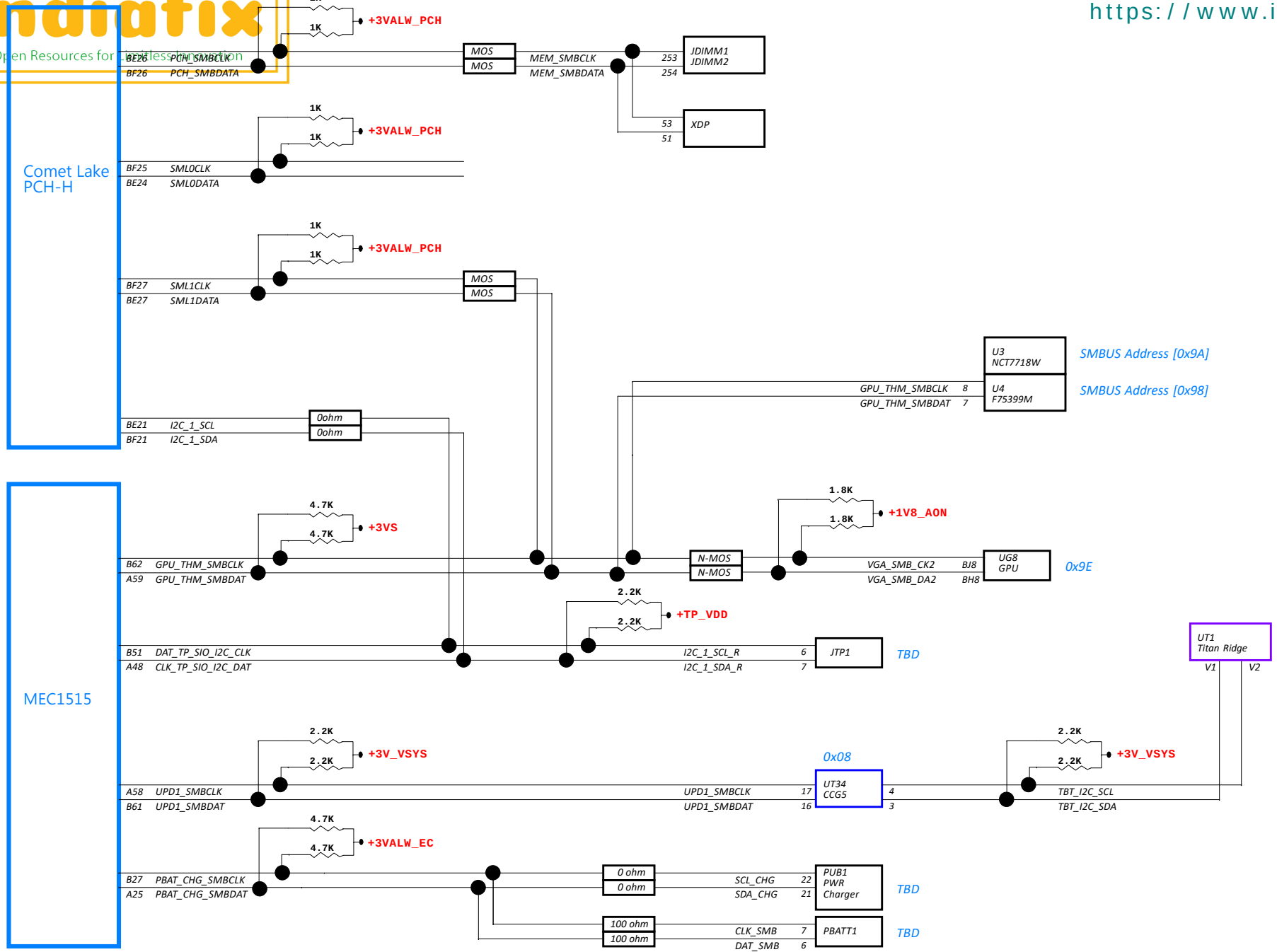

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Compal Electronics, Inc.

Title: **SMBus Block Diagram**

Size	Document Number	Rev
	LA-L652P	1.0(A00)

Date: Wednesday, December 15, 2021 Sheet 61 of 120

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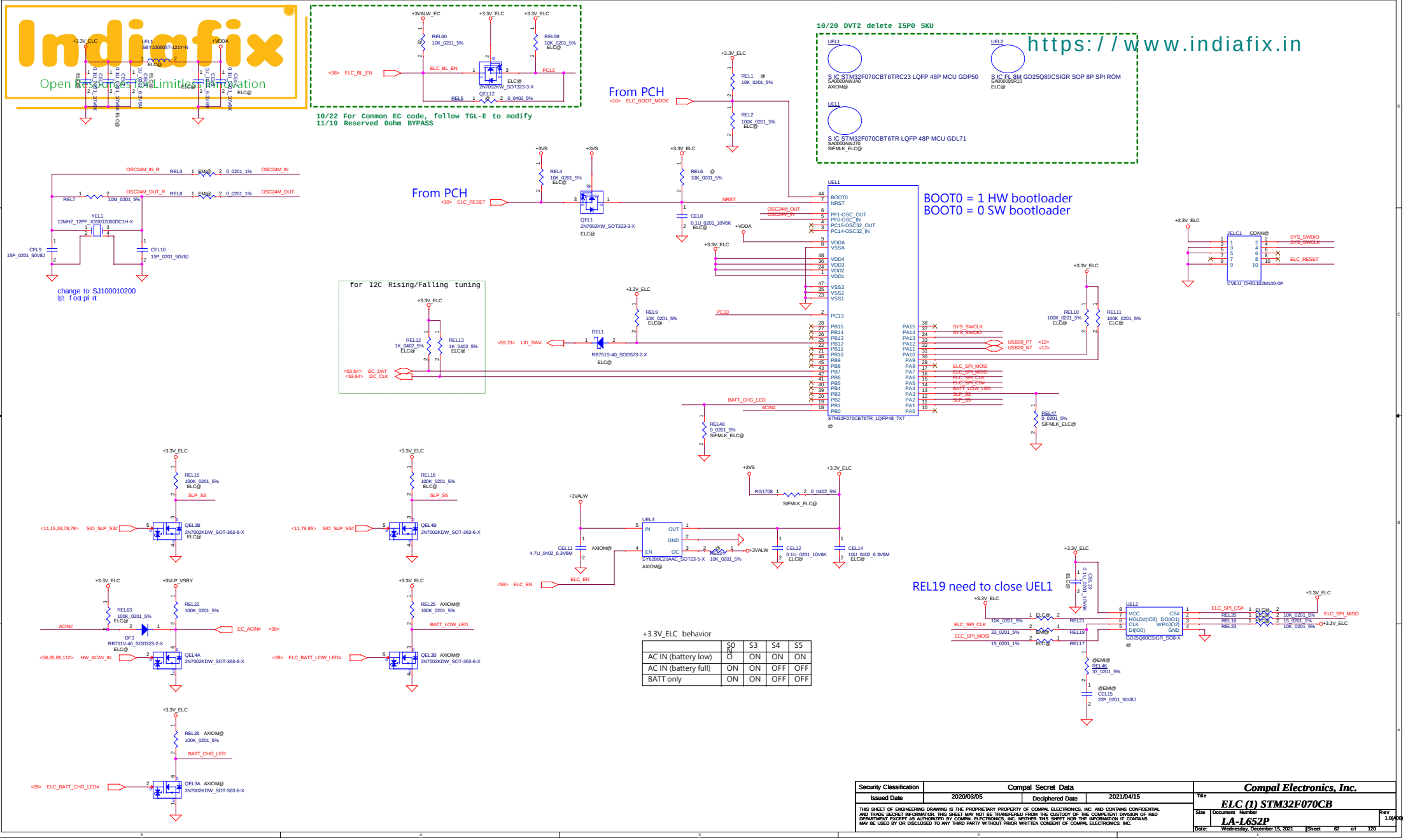

	S0	S3	S4	S5
AC IN (battery low)	O	ON	ON	ON
AC IN (battery full)	ON	ON	OFF	OFF
BATT only	ON	ON	OFF	OFF

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Issued Date	2020/03/05	Deciphered Date	2021/04/15	Title: ELC (1) STM32F070CB
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			Date: Wednesday, December 15, 2021 Sheet 62 of 120

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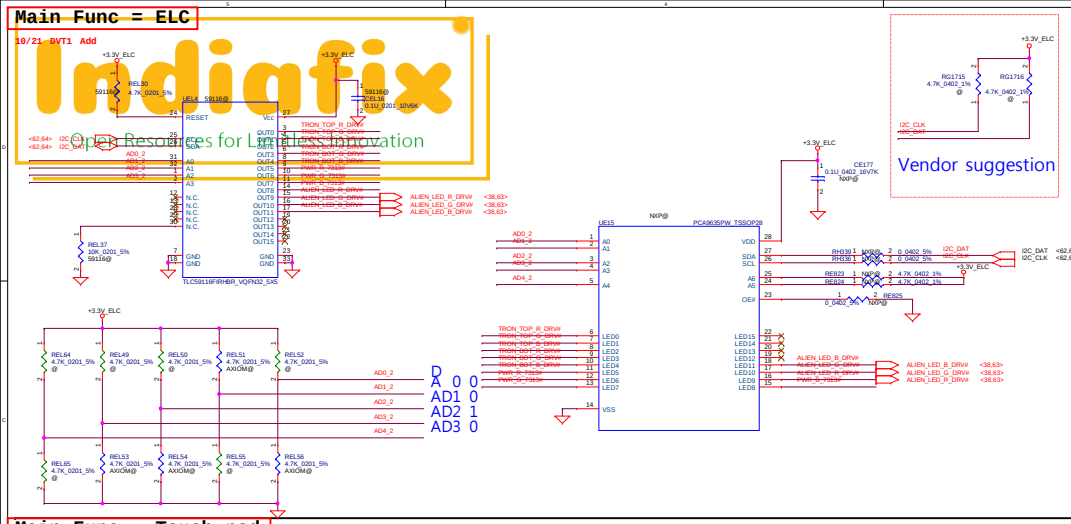
Main Func = ELC

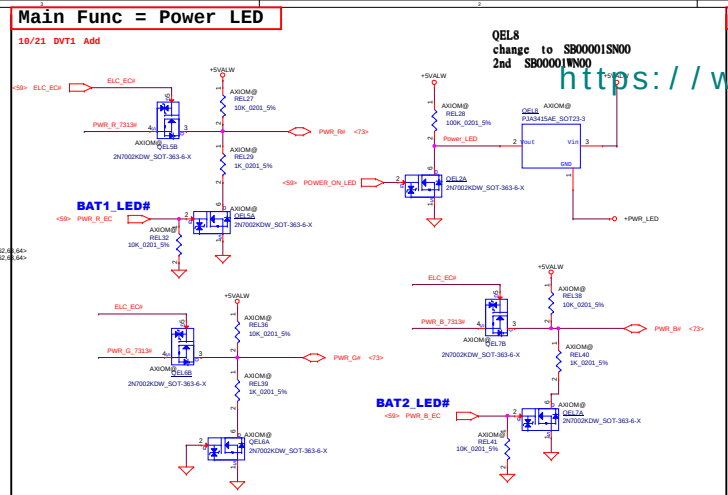
10/21 DVT1 Add



Main Func = Power LED

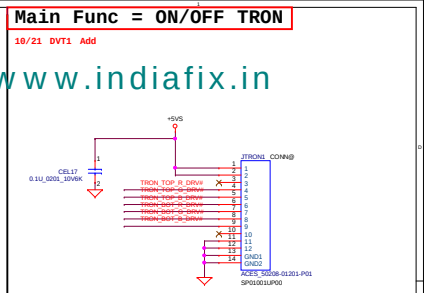
10/21 DVT1 Add

QEL8 change to SB00001SN00
2nd SB00001WN00

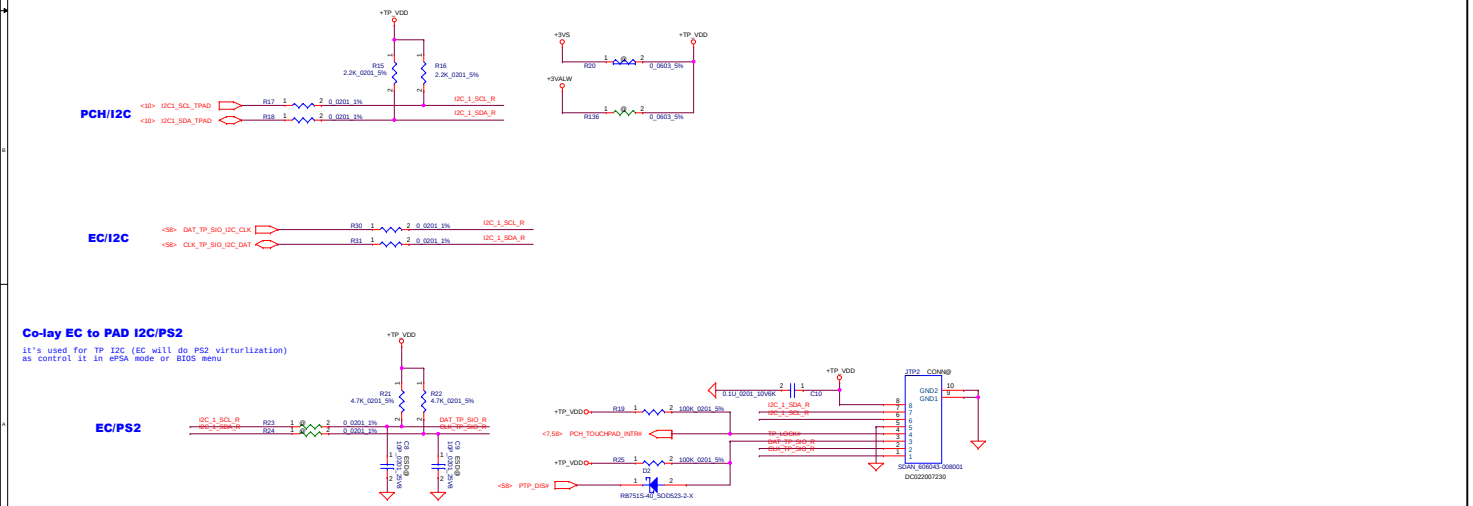


Main Func = ON/OFF TRON

10/21 DVT1 Add



Main Func = Touch pad

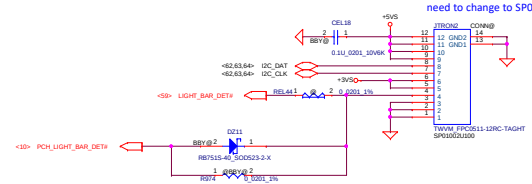


Co-lay EC to PAD I2C/PS2

it's used for TP I2C (EC will do PS2 virturlization) as control it in ePSA mode or BIOS menu

Main Func = Primax Front Lighting

need to change to SP01002TZ00



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Issued Date	2020/03/05	Deciphered Date	2021/04/15
Title	ELC (2) TP/PWR/TRON		
Size	Document Number		Rev
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Main Func = KB/KBBL

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CAP LED Control
LOW actived from KBC GPIO

SB00001H300

0713 add from EC

Fuse add on MCU/B side

10/21 DVT1 Add

10/21 DVT1 Add

PD on MCU/B side

follow E board 0526

8/17 modify BOM config of the diode for ESD request

Keyboard Backlight

KB Backlight Power Consumption: 400mA max.

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Issued Date	2020/03/05	Deciphered Date	2021/04/15

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Compal Electronics, Inc.

Title: **MCU Per Key/4 Zone KB**

Size | Document Number: **LA-L652P** | Rev: 1.0(400)

Date: Wednesday, December 15, 2021 | Sheet 64 of 120

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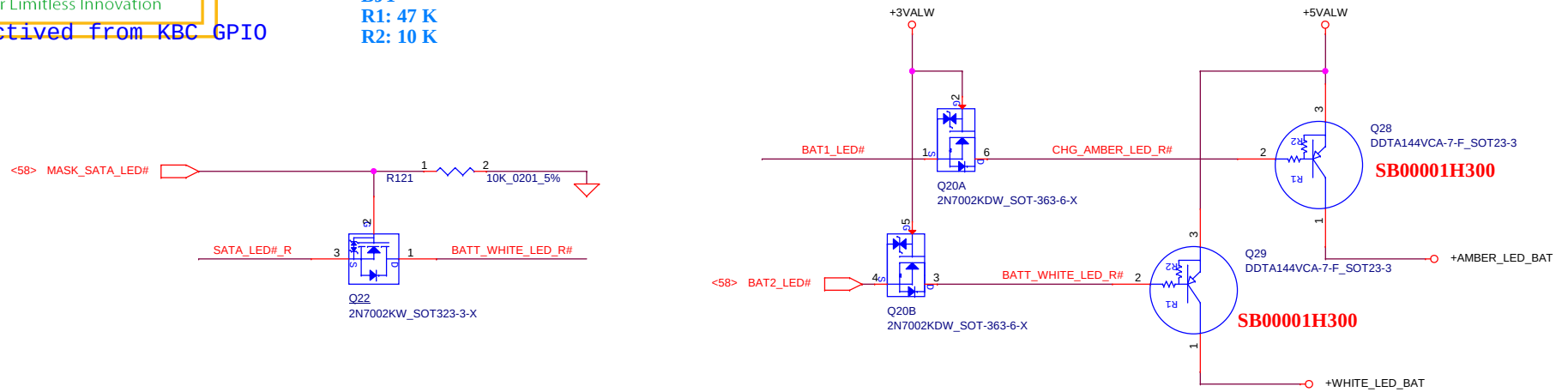
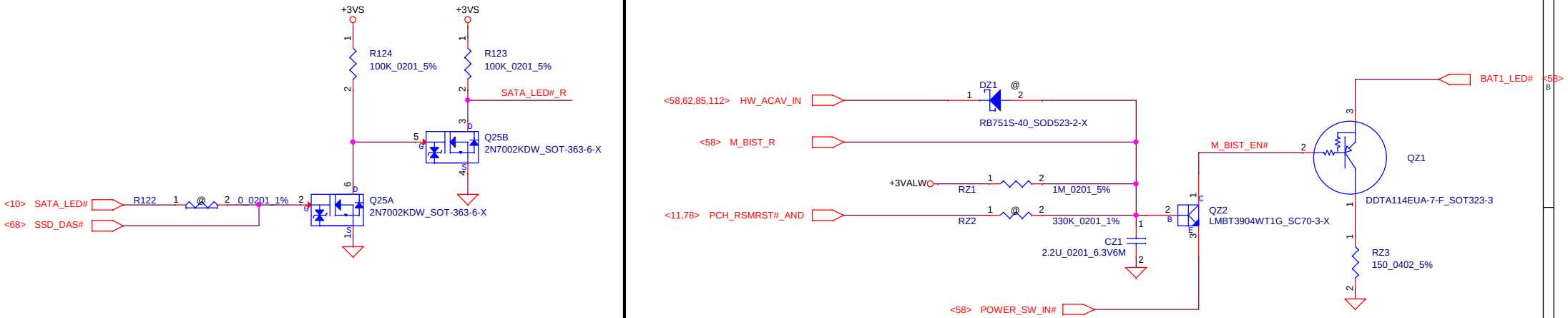
Main Func = Battery LED

Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K



Main Func = M_BIST



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Issued Date	2020/03/05	Deciphered Date	2021/04/15

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Title	LED (SIF)		
Size	Document Number		Rev
	LA-L652P		1.0(400)
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Main Func = RTC Gen9

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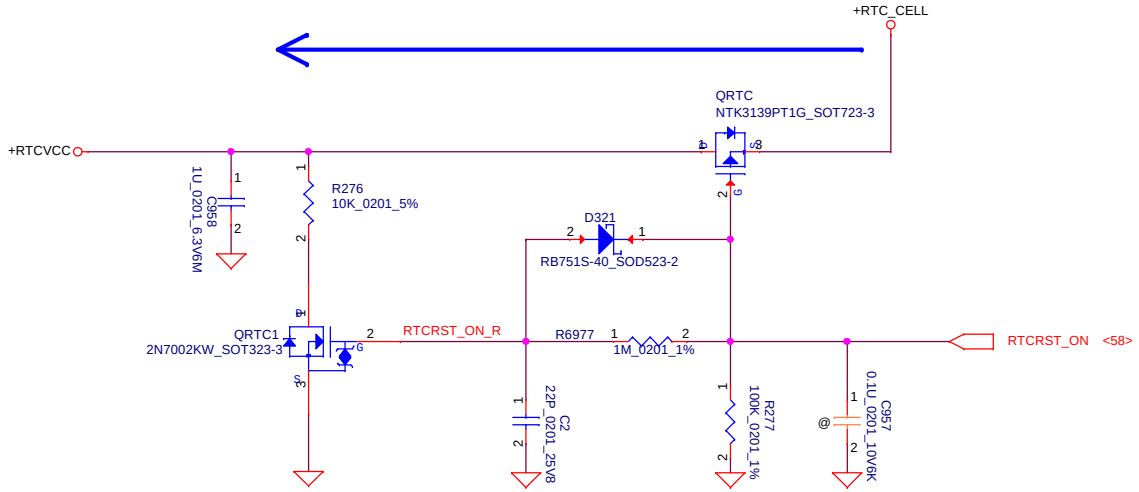
Default: OD EC drives GPIOs to LOW to turn ON power to VCCRTC.



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Title: RTC Gen9			
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Size	Document Number: LA-L652P	Rev: 1.0(400)
Date: Wednesday, December 15, 2021	Sheet 67 of 120	

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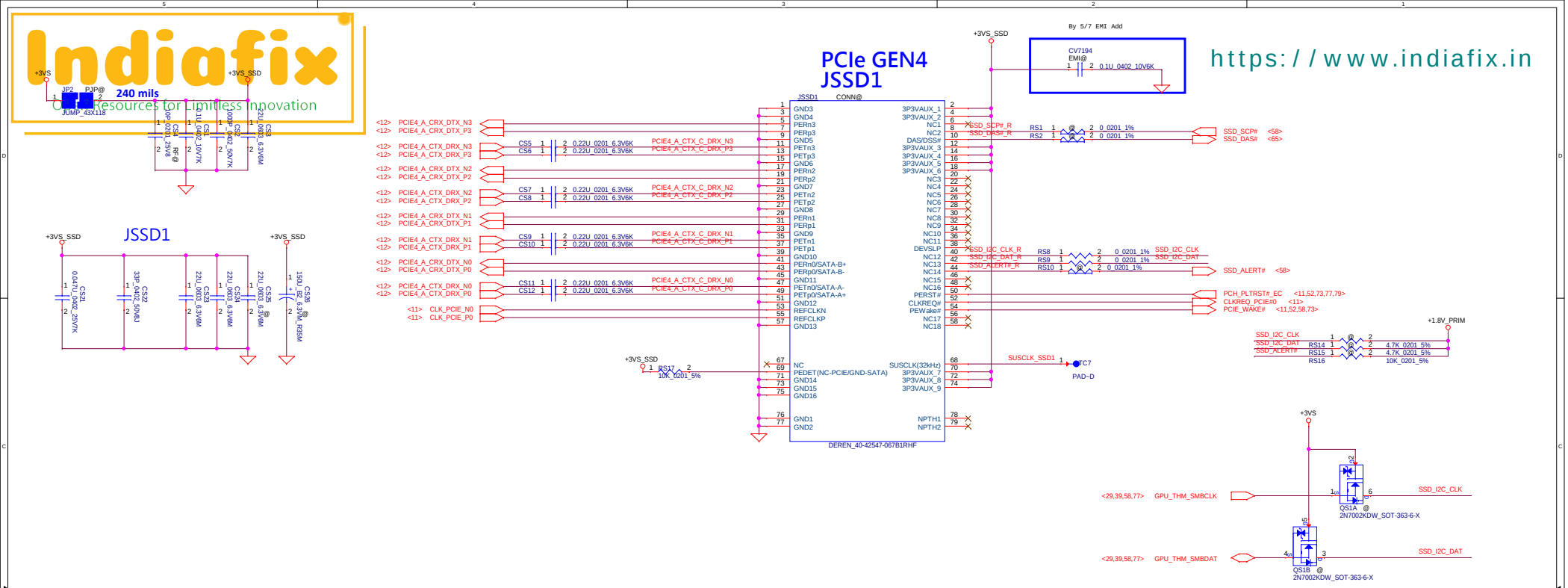
PCIe GEN4 JSSD1



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Compal Electronics, Inc.

Title: **NGFF SSD x2**

Size	Document Number	Rev
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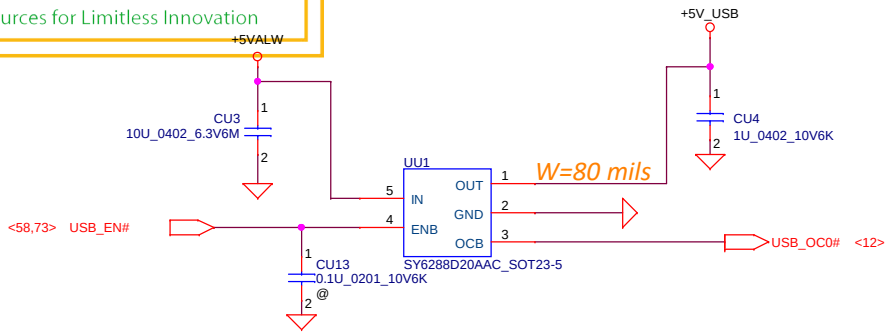

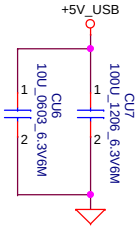

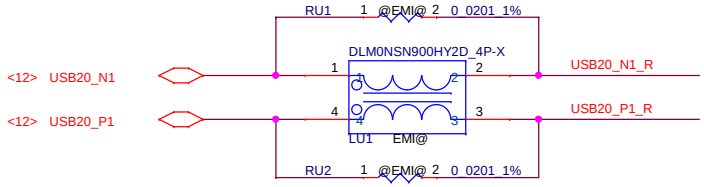

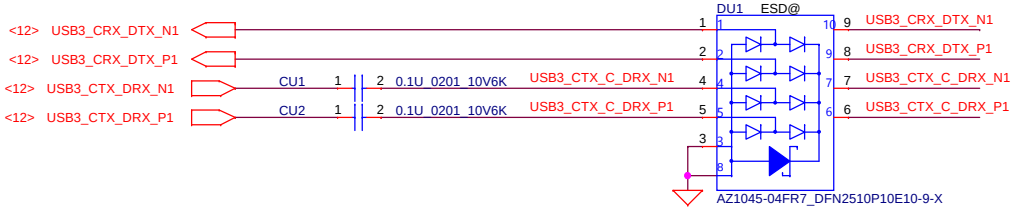

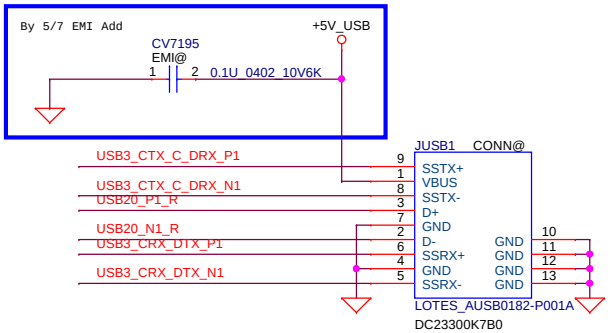

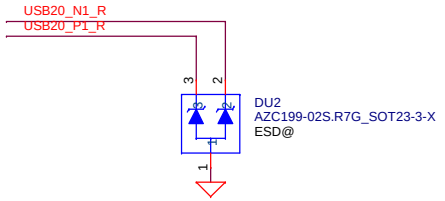

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Title: **USB3.1 TypeA Gen1**

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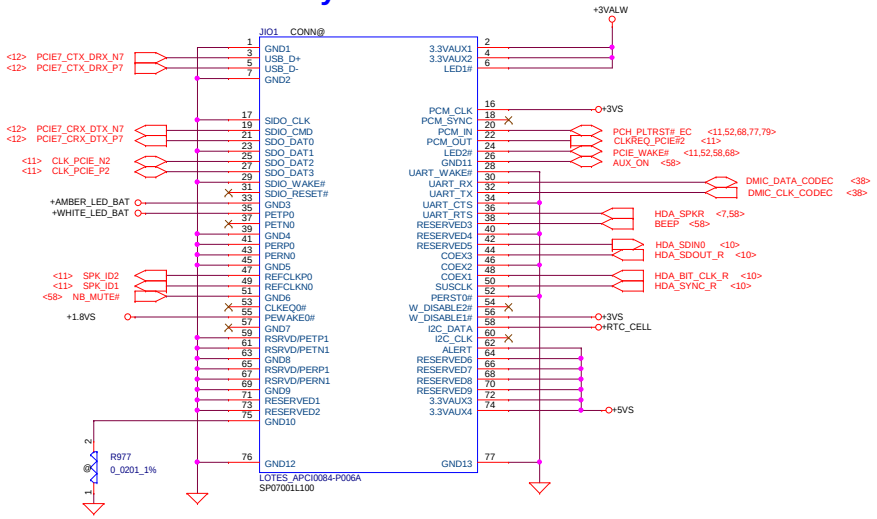
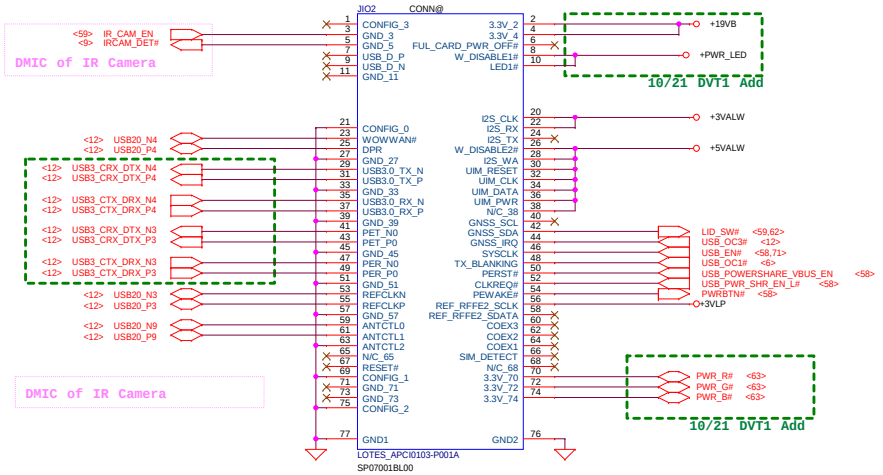
A Key CONN

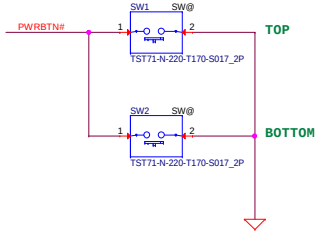


For LAN DB CONN (LEFT)

B Key CONN



For USB DB CONN (RIGHT)



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Compal Electronics, Inc.

Title: **IO Board CONN**

Size	Document Number	Rev
	LA-L652P	1.0(A00)

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Title: DOCK(RSVD)			
Size	Document Number: LA-L652P		Rev: 1.0(400)
Date: Wednesday, December 15, 2021	Sheet 74 of 120		

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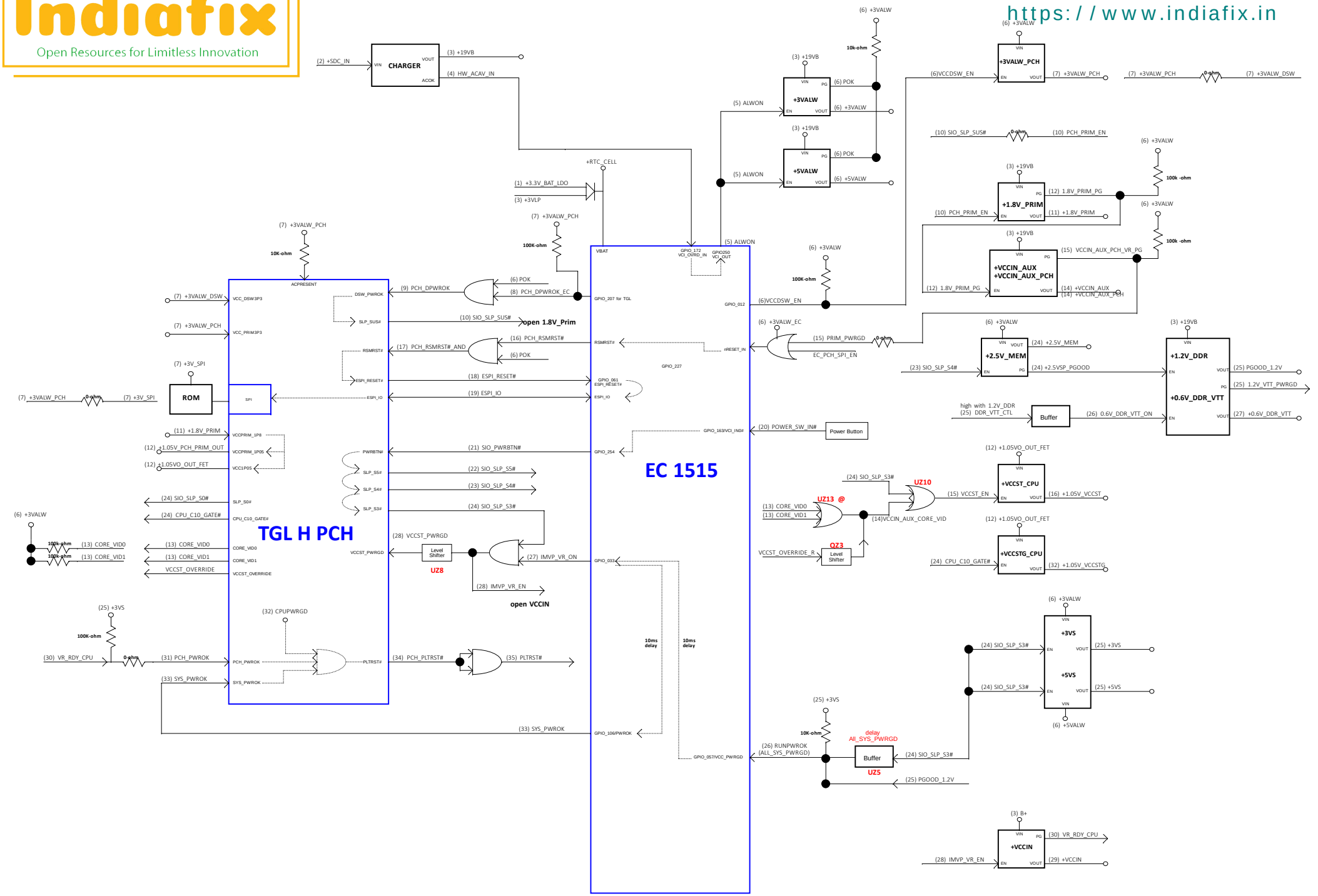

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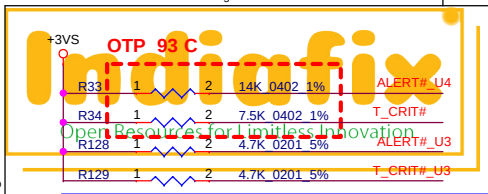
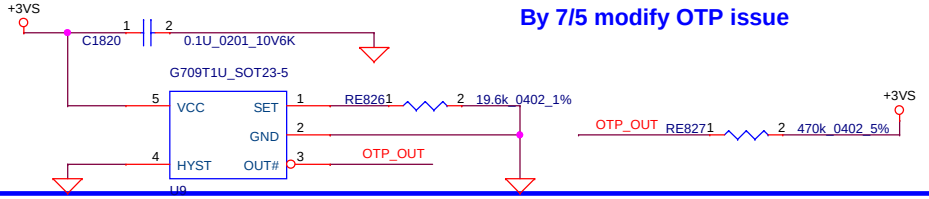


By 7/5 modify OTP issue



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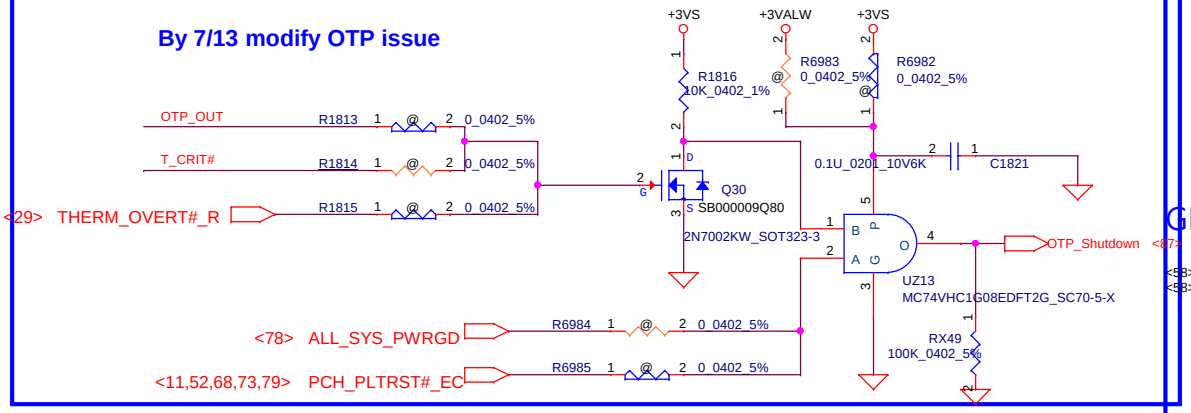

By 5/25 modify P board 5V ONLY

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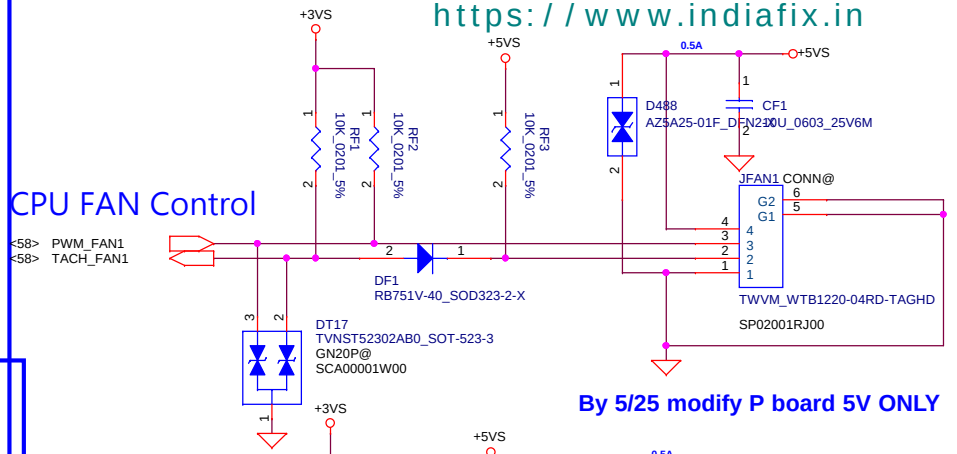
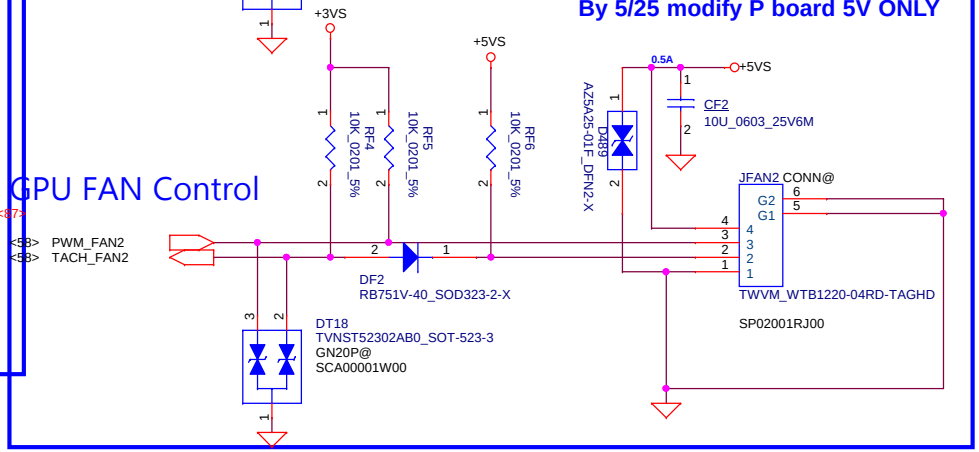
CPU FAN Control

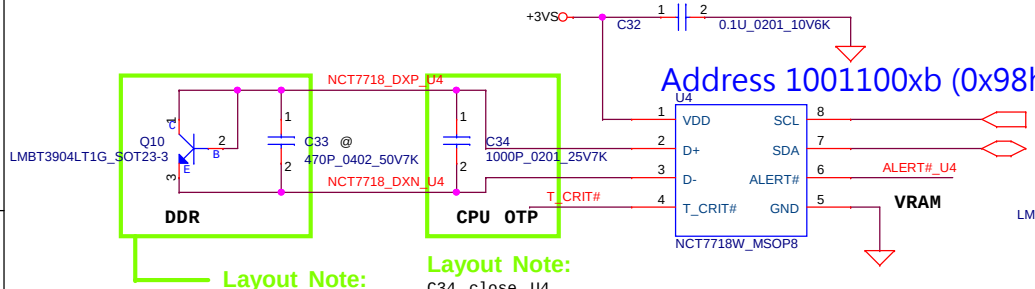


By 5/25 modify P board 5V ONLY

GPU FAN Control



Address 1001100xb (0x98h)

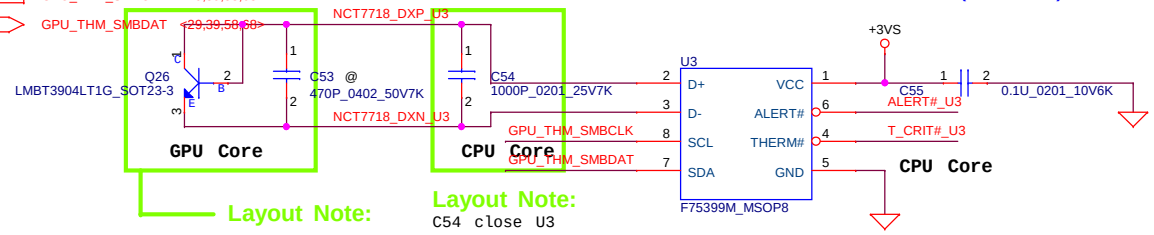


Layout Note:

Layout Note:
C34 close U4

DXN and DXP routing width and spacing is 10 mil / 10 mil.

Address 1001101xb (0x9Ah)



Layout Note:

Layout Note:
C54 close U3

DXN and DXP routing width and spacing is 10 mil / 10 mil.

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2021/04/15

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Compal Electronics, Inc.

Title: **FAN/Thermal**

Size | Document Number: **LA-L652P** | Rev: 1.0(400)

Date: Wednesday, December 15, 2021 | Sheet 77 of 120

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Main Func = DC/DC

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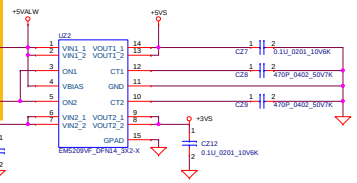
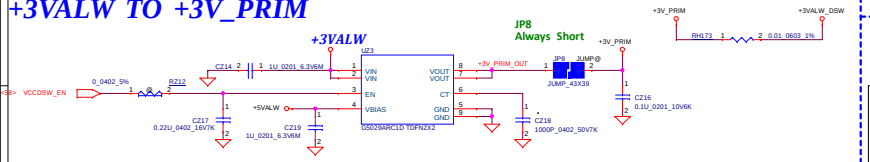
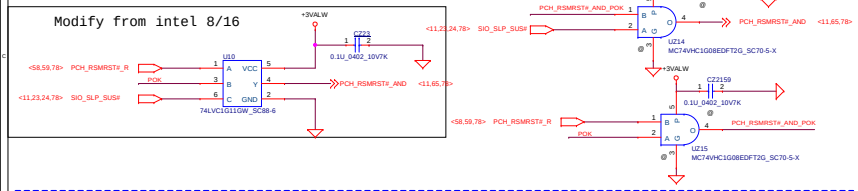
+5VS / +3VS for System

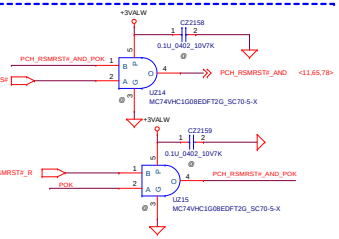


+3VALW TO +3VALW_DSW
+3VALW TO +3V_PRIM

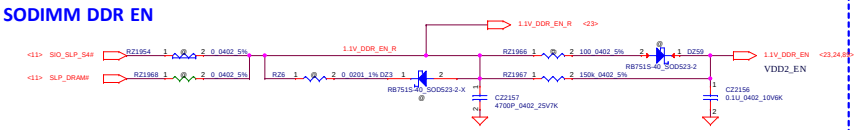


RSMRST circuit

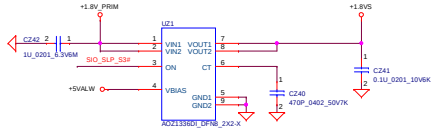




SODIMM DDR EN

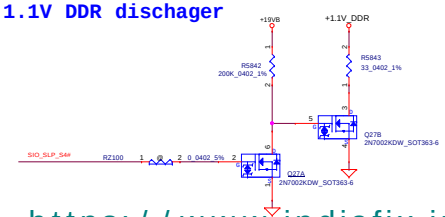


+1.8VS for System



+1.1V

1.1V DDR dischager



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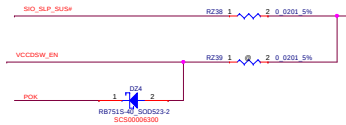
Sequence Logic

11/4 DVT1 modify for material preparat i on
SC100000S00 change to SCS00006300

https://www.indiafix.in

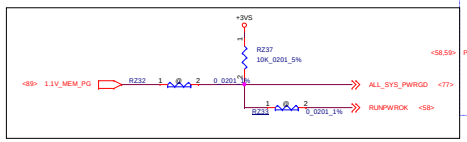
Enable +1.2V_DDR



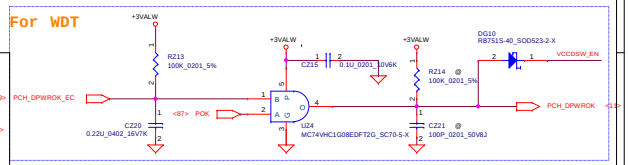
Enable +1.8V_PRIM

IMVP_VR_ON&VCCST_PWRGD

For V tree

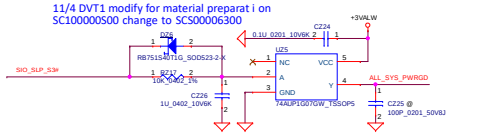


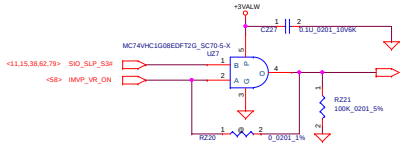
For WDT



Buffer with Open Drain Output For ALL_SYS_PWRGD

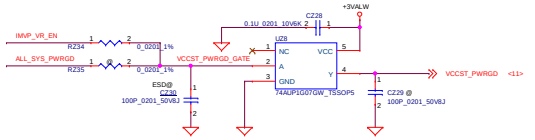
11/4 DVT1 modify for material preparat i on
SC100000S00 change to SCS00006300



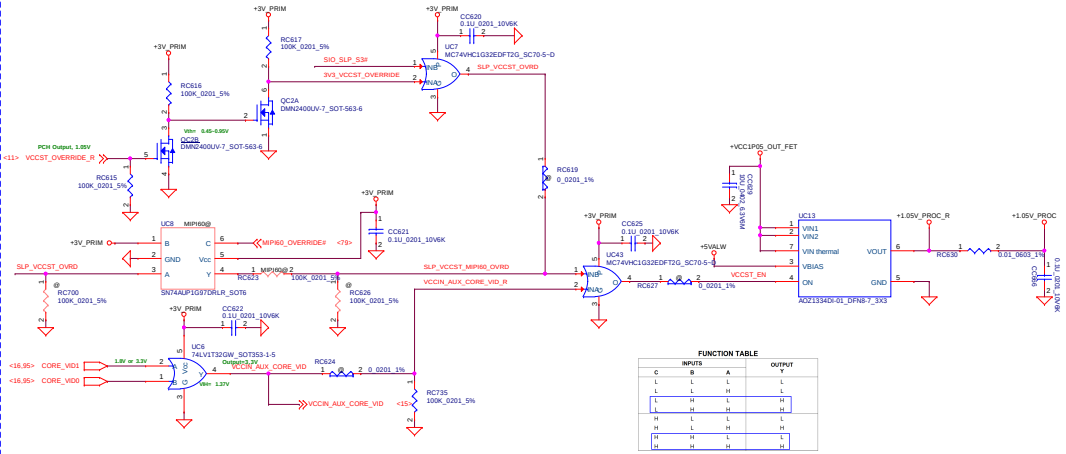


11/4 DVT1 modify for material preparat i on
SA00000OH00 change to SA0000BIP00

Buffer with Open Drain Output For H_VCCST_PWRGD



+1.05V_PROC



FUNCTION TABLE

INPUTS			OUTPUT
C	B	A	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

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Compal Electronics, Inc.

Title: DC/DC Interface

Size	Document Number	Rev
	LA-L652P	1.0(0.0)

Date: Wednesday, December 15, 2021 | Sheet 78 of 120

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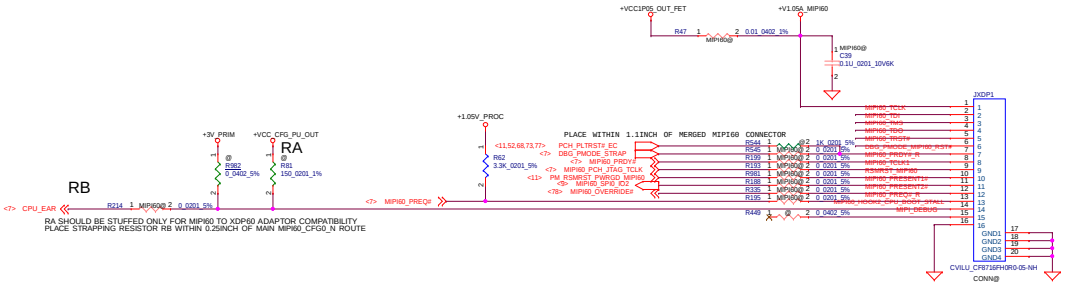
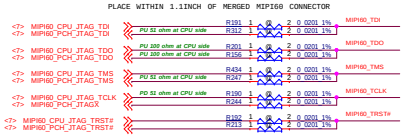




CFG Config

CFG2

PEG x16 Lane reversal

0: Reversal

1: Non-Reserval

CFG4

eDP enable strap

0 : enable

1 : disable

CFG5, CFG6

PCIE16 Port Bifurcation - CGF[6:5]

11 : x16 (Default)
10 : x8, x8
01 : Reserved
00 : x8,x4,x4

CFG14

PCIE4 Lane Reversal

0 : Reseved

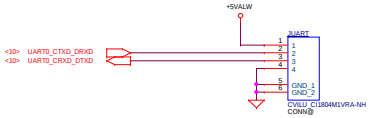
1 : Normal (default)

Power Monitor

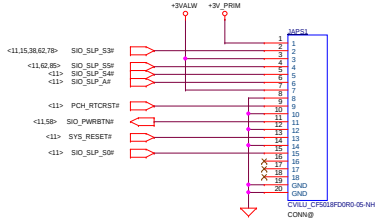
2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+

P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19

BIOS UART Debug



APS



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Issued Date	2020/03/05	Deciphered Date 2021/04/15	Title: Debug APS,DEG
			Size: Document Number: LA-I652P Rev: 1.0(0.0)
			Date: Wednesday, December 15, 2021 Sheet 78 of 130

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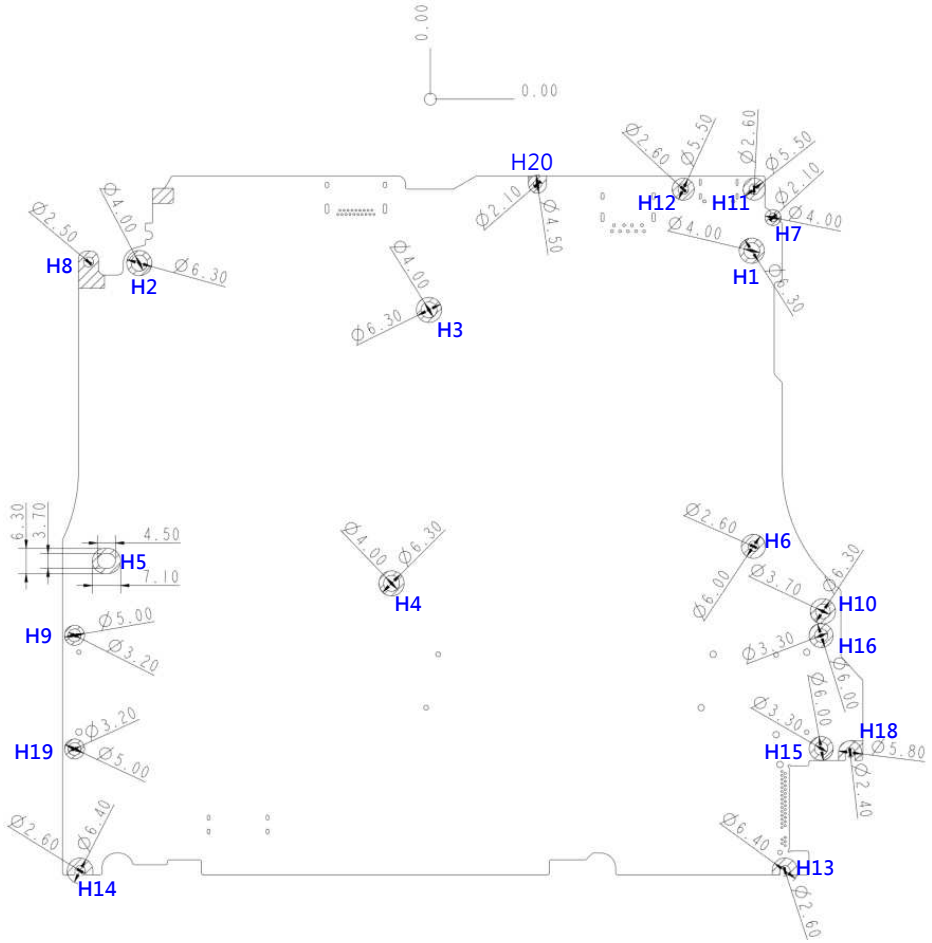

CPU & GPU

H1 H_4P0-G-V
H2 H_4P0-G-V
H3 H_4P0-G-V
H4 H_4P0-G-V
H5 H_4P5X3P7
H6 H_2P6-G-V

PTH

H7 H_2P1-G-V
H8 H_2P5-G-V
H20 H_2P1-G-V
H10 H_3P7-G-V
H11 H_2P6-G-V
H12 H_2P6-G-V
H13 H_2P6-G-V
H14 H_2P6-G-V
H18 H_2P4-G-V

Stand-off

H15 H_3P3
H16 H_3P3
H9 H_3P2
H19 H_3P2

Fiducial Mark

FD1 @FIDUCIAL
FD2 @FIDUCIAL
FD3 @FIDUCIAL
FD4 @FIDUCIAL
FD5 @FIDUCIAL
FD6 @FIDUCIAL
FD7 @FIDUCIAL
FD8 @FIDUCIAL

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Compal Electronics, Inc.

Title: **Screw Hole**

Size | Document Number: **LA-L652P** | Rev: 1.0(A00)

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Power block

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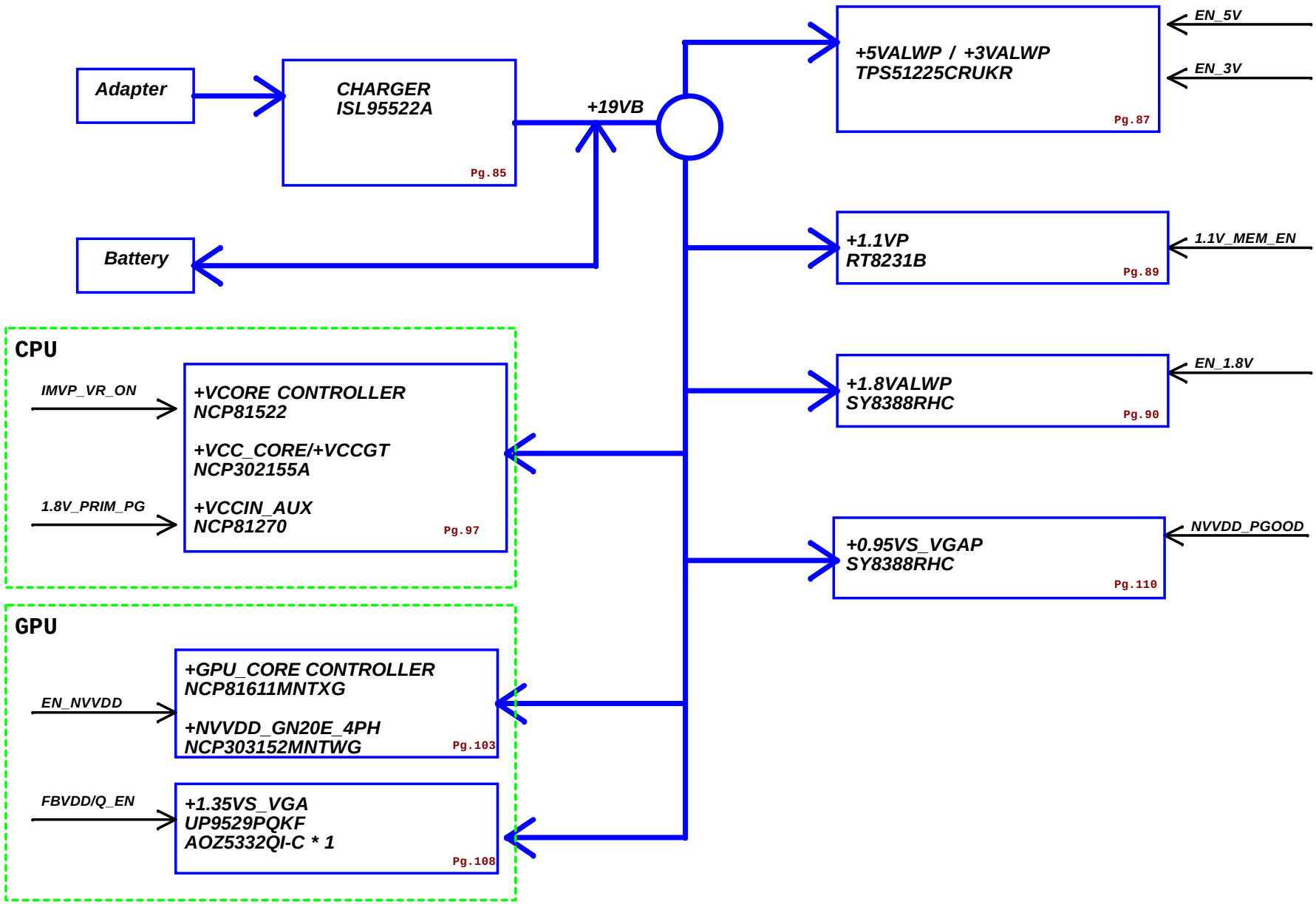

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Compal Electronics, Inc.

Title: PWR_POWER BLOCK DIAGRAM

Size | Document Number: LA-L652P | Rev: 1.0(400)

Date: Wednesday, December 15, 2021 | Sheet 81 of 120

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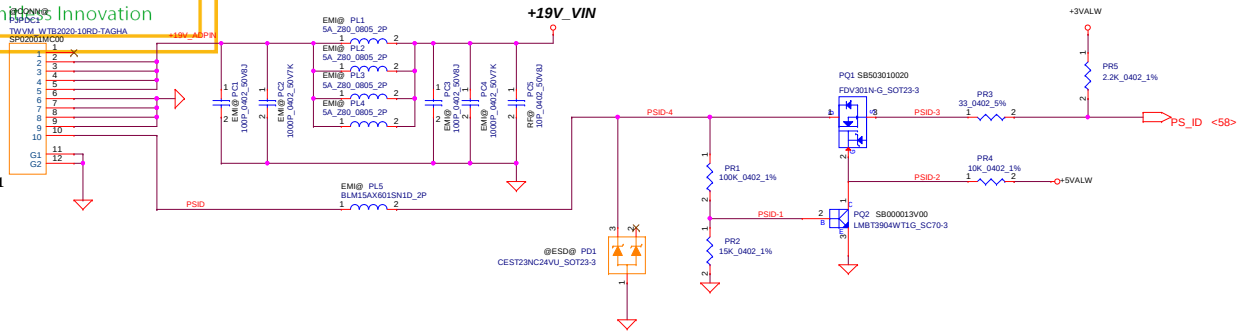
Main Func = DCIN CONN

Adapter Connector

Adapter Bot Side

PIN1 N/A
PIN2 ADPIN
PIN3 ADPIN
PIN4 ADPIN
PIN5 ADPIN
PIN6 GND
PIN7 GND
PIN8 GND
PIN9 GND
PIN10 PSID
ACES_50459-010H0M0-001

Adapter 180W
180W / 19V=9.47A



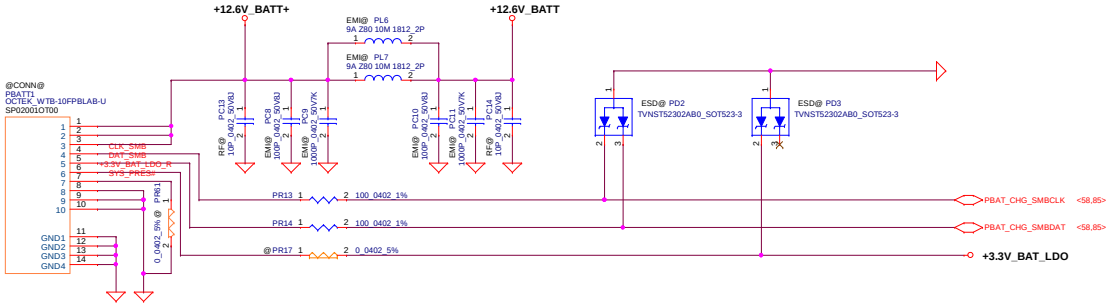
Main Func = BATT CONN

Battery Connector

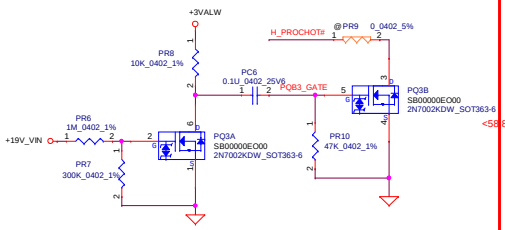
Battery Bot Side

PIN10 GND
PIN09 GND
PIN08 GND
PIN07 SYS_PRES#
PIN06 BATT_PRS#
PIN05 DAT_SMB
PIN04 CLK_SMB
PIN03 BATT+
PIN02 BATT+
PIN01 BATT+
SP07001R500

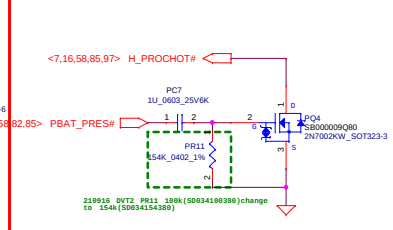
Battery 56W
56W/11.4V=4.91A
Battery 86W
86W/11.4V=7.54A

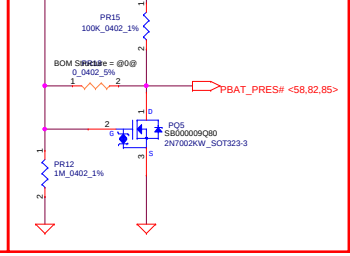


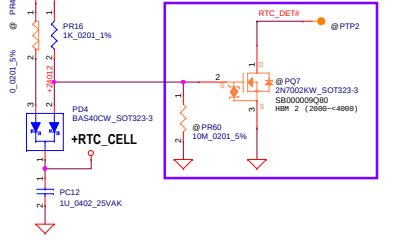
Adapter protection:



Battery protection:







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Compal Electronics, Inc.

Title: PWR-DCIN / OTP / BATT CONN / RTC

Size: | Document Number: LA-L652P | Rev: 1.0(ADD)

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Title			
Size	Document Number		Rev
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Compal Electronics, Inc.			
Title			
Size	Document Number		Rev
	LA-L652P		1.0(ADD)
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Main Func = CHARGER

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+12.6VB_VCHGR
Vout=11.4V(Typ)
IDC=11.45A(quick charge 1.5C)
8.39A(discharge 1.1C)

OCP current A
FSW=796kHz

	TYP	MAX
H/S Rds(on)	4 mohm	5.2 mohm
L/S Rds(on)	4 mohm	5.2 mohm

+19V_VIN
+19VB
+12.6V_BATT_R
+12.6V_BATT

Main: MAG. LAYERS
Package: 11.5 x 10.3 x 3
Idc=13A, Isat=16A
Rdc=8mohm
SH000000XV00

Delay adaptor OC H_PROCHOT#
2ms while hybrid power transition

VDD_CHG +3VALW

	CPN	Value	Effective capacitance	Renesas recommend
DCIN	SE000013880	4.7uF_0603_25V	0.4uF	0.4uF
VDD	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
VDDP	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
CBOOT	SE000005Z80	0.22U_0603_25V7K	0.15uF	0.15uF

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Issued Date	2020/03/05	Deciphered Date	2021/04/15

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Compal Electronics, Inc.
Title: PWR_CHARGER
Size: | Document Number: IA-L652P | Rev: 1.0(400)
Date: Wednesday, December 15, 2021 | Sheet 85 of 120

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Main Func = 3.3VALWP / 5VALWP

Input Current: 12.76A
3.4V*9.7A/0.85/9V=3.58A
5.16V*13.61A/0.85/9V=9.18A

3.3VALWP
Vout=3.4V
TDC 8.05A
Peak Current 11.5A
OCP current 14.95A
OVP=3.824V~3.994V(112.5%~117.5%)
UVP=1.869V~2.209V(55%~65%)
FSW=355kHz

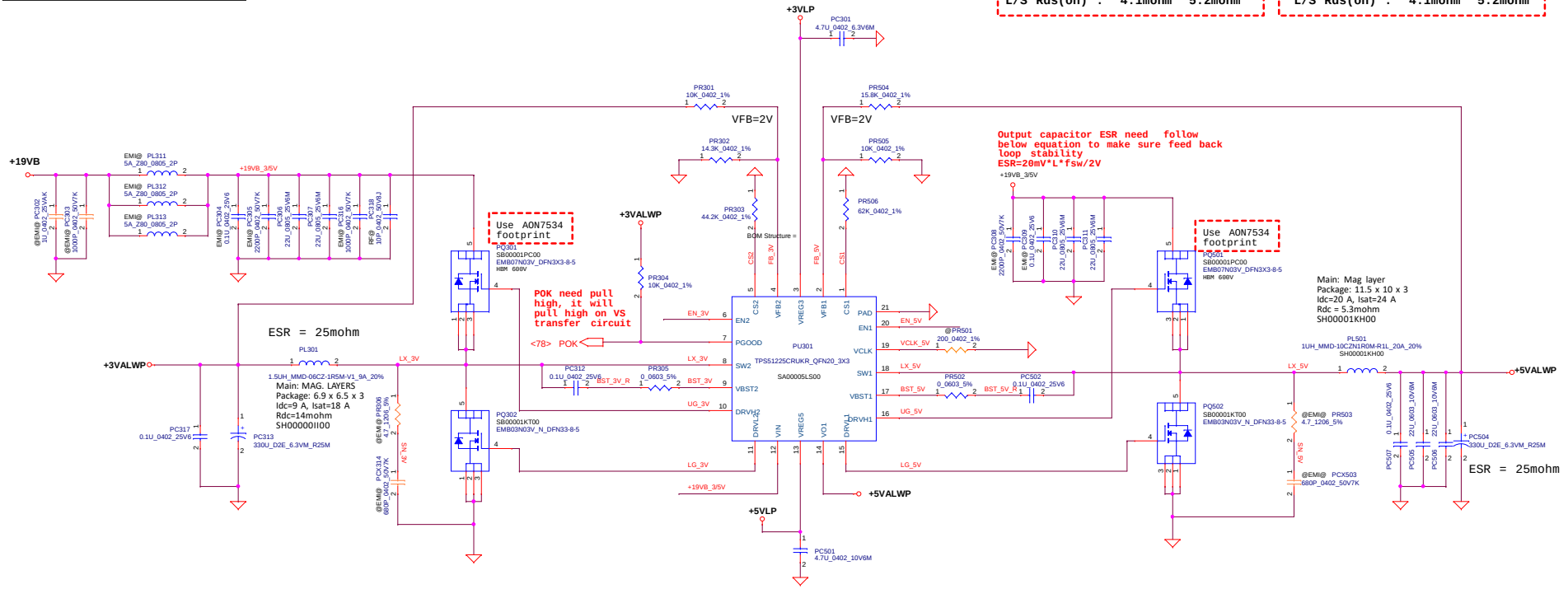
MOS (VGS = 4.5V)

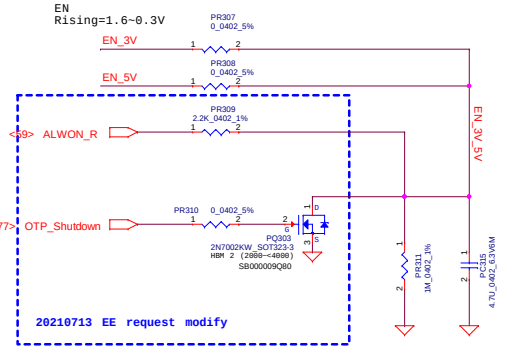
	TYP	MAX
H/S Rds(on) :	6.7mohm	8.5mohm
L/S Rds(on) :	4.1mohm	5.2mohm

5VALWP
Vout= 5.16V
TDC =13.61A
Peak Current 17A
OCP current 22.1A
OVP=5.805V~6.063V(112.5%~117.5%)
UVP=2.838V~3.354V(55%~65%)
FSW=300kHz

MOS (VGS = 4.5V)

	TYP	MAX
H/S Rds(on) :	6.7mohm	8.5mohm
L/S Rds(on) :	4.1mohm	5.2mohm



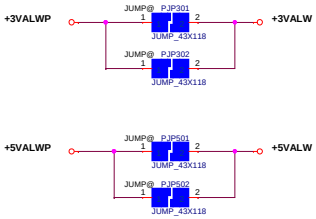


	ALWON	+5VALWP	+3VALWP
S5	H	on	on
S3	H	on	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

OTP_Shutdown	+5VALWP	+3VALWP
L	off	off

Note: OTP_Shutdown for thermal protection



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Compal Electronics, Inc.

Title: PWR_+3.3VALWP/+5VALWP

Size | Document Number: LA-L652P | Rev: 1.0(ADD)

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Main Func = +1.1VP

Input Current: 0.265

1.113V*1.82A/0.85/9V=0.265A

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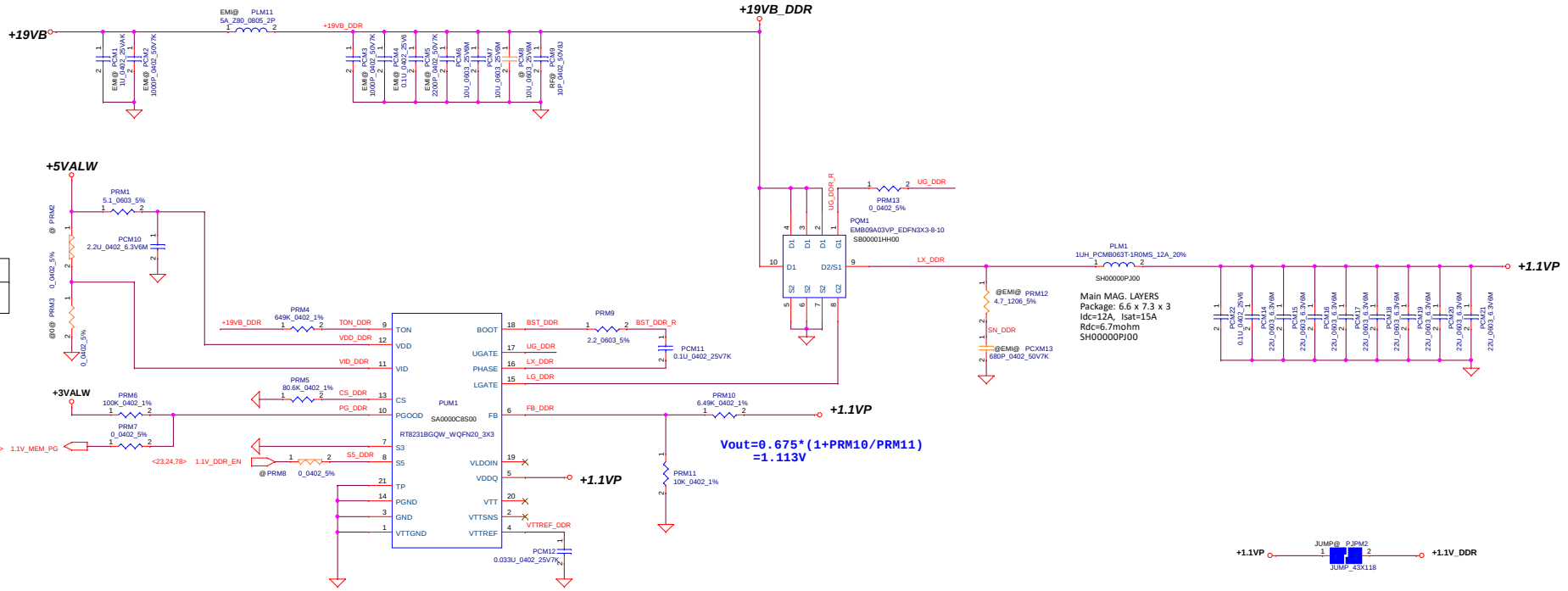
+1.1VP
Vout= 1.113V
IDC 1.82A
Peak Current 2.6A
OCP current 3.12A
OVP=1.22V~1.34V(110%~120%)
UVP=0.4V~0.5V
FSW= 400K Hz

MOS (VGS = 4.5V)

	TYP	MAX
H/S Rds(on) :	11 mohm	13 mohm
L/S Rds(on) :	11 mohm	13 mohm

VID	Vref
High	0.675V
Low	0.75V



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Compal Electronics, Inc.

Title: PWR_1.2VP/0.6VSP/+2.5V

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Main Func = 1.8VALWP

Input Current: 0.73A
1.8V*3.1A/0.85/9V=0.73A

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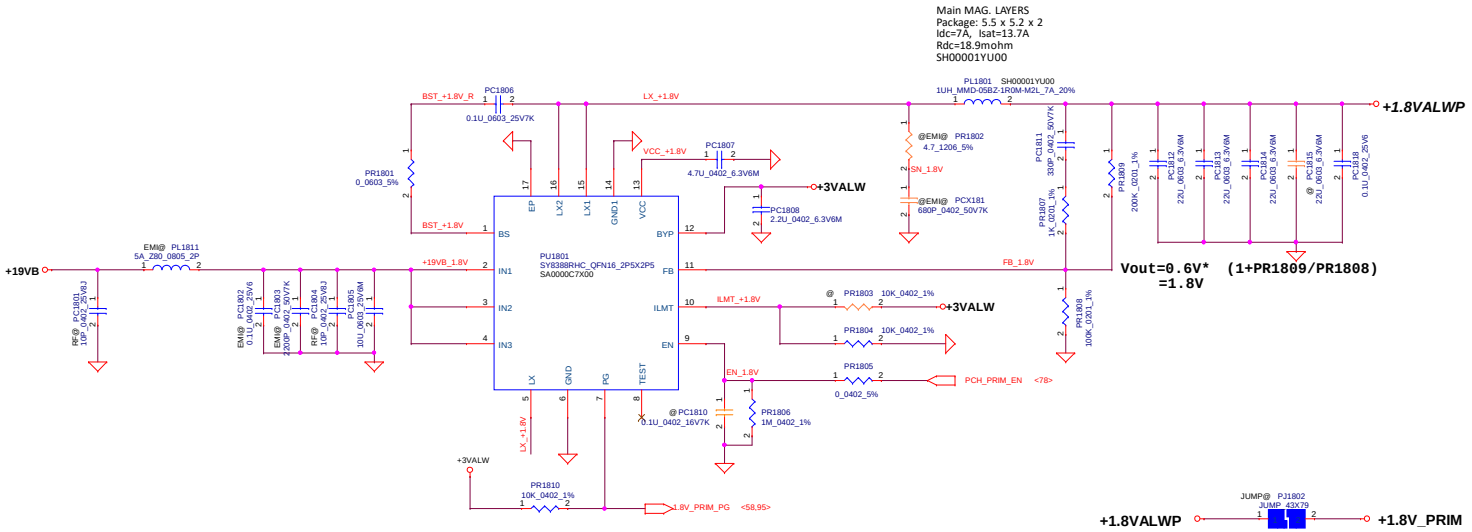
+1.8VALWP
IOC = 3.1A
Peak Current = 4.45 A
OVP=2.106V~2.214V(117%~123%)
OCP=8A
UVP=0.99V~1.17V(55%~65%)
FSW= 500K Hz



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Title: PWR-+1.8V

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Main Func = +VCCIN_AUX

Input Current: 4.24A
1.8V*18A/0.85/9V=4.24A

+19VB → EMI@ PLA11 5A_Z80_0805_2P → +19VB_AUX
EMI@ PLA12 5A_Z80_0805_2P

+VCCIN_AUX
Vout 1.8V
IPU2(fDC) 18A
Peak Current = 33A(ICCmax)
OCP 42.9 A
FSW= 600KHz

MOS (VGS = 4.5V)

	TYP	MAX
Rds(on) :	5.2 mohm	7 mohm

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+3VALW
+19VB_AUX
+5VALW
+VCCIN_AUX

Need to calculate Vin ripple

Main: MAG LAYERS
Package: 6.86x 6.47 x 4
Idc=32A, Isat=55A
Rdc=0.98mohm +/-5%
SH00001G400

PLA1 0.22UH_MMD-06DZER22MEM2L__32A_20%

PQA1 AOE6930_DFN5X6E8-10 HBM 500V

PUA1 NCP81270MNTXG_QFN20_4X4 SA0000EFV10

Place close to PLA1
Place near to VRM

R_DOSC=2K, Fsw=300KHZ
R_DOSC=6K, Fsw=400KHZ
R_DOSC=15K,Fsw=600KHZ

VID1_VID0 =00, Vo=0V
VID1_VID0 =01, Vo=1.1V
VID1_VID0 =10, Vo=1.65V
VID1_VID0 =11, Vo=1.8V

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Main Func = +VCCIN_AUX DECOUPLING

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Follow Intel ADL-P PDG Rev1.0
+VCCIN_AUX Output CAP :

CPU Primary Side:
330uF *1pcs
47uF_0603 *4 pcs

CPU Secondary side:
10uF_0402 *10pcs
47uF_0603 *4pcs

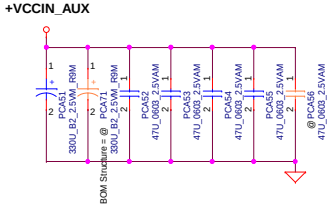
Compal
+VCCIN_AUX Output CAP :

CPU Primary Side:
330uF_B2_2.5V_R9M *1pcs
47uF_0603_2.5V_X6S *5 pcs(1pcs reserved)

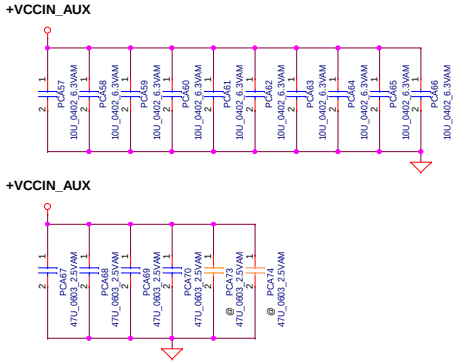
CPU Secondary side:
10uF_0402_6.3V_X6S *10pcs
47uF_0603_2.5V_X6S *4pcs

For FIVR solution
CPU Primary Side:
47uF_0603 *1
Placeholder 0402 *1
on EE side

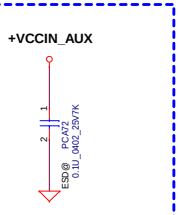
CPU Primary Side



CPU Secondary side



5/6 ESD Oliver requirement to add



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Title

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Main Func = CPU (IA/GT)
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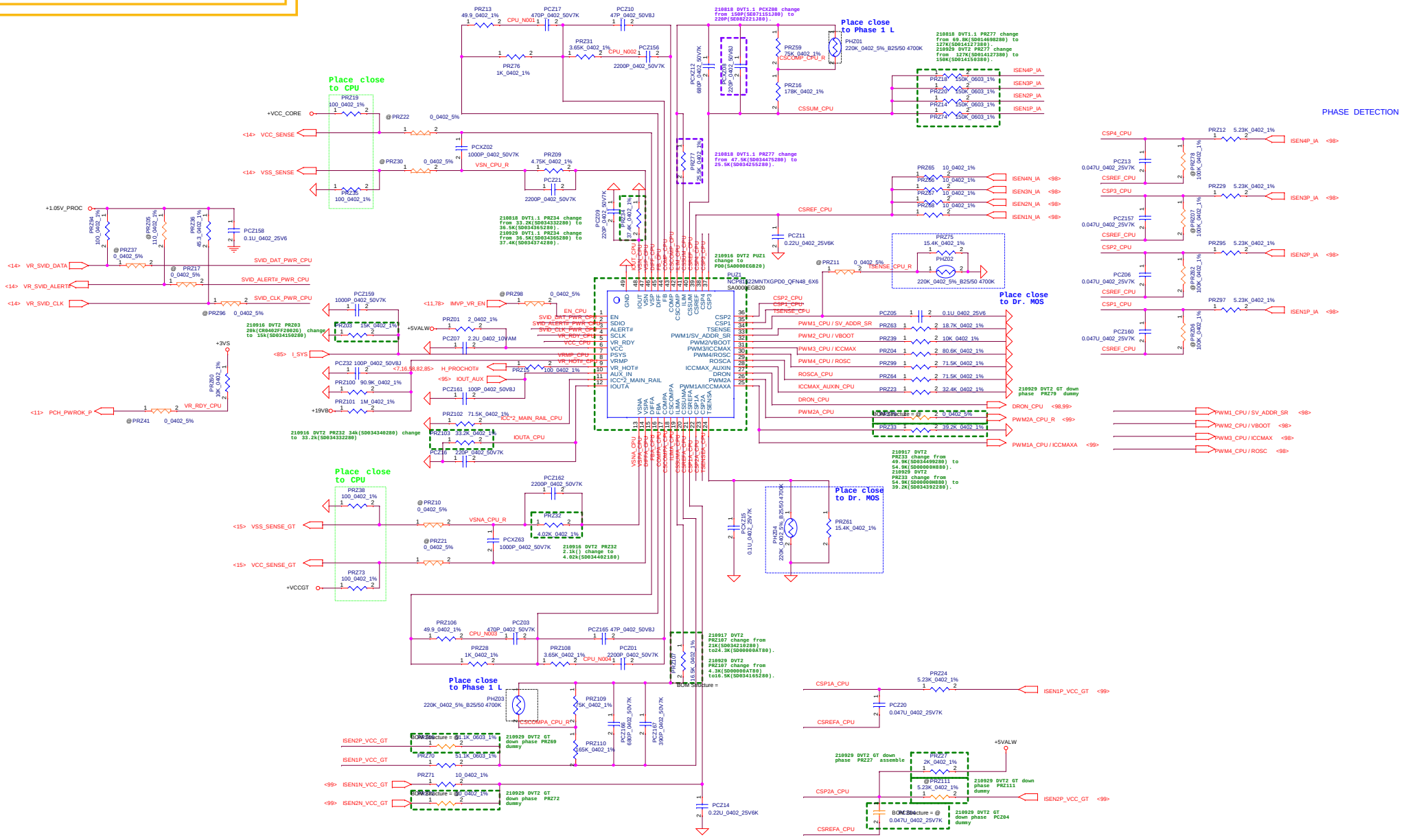

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Main Func = +VCCCORE

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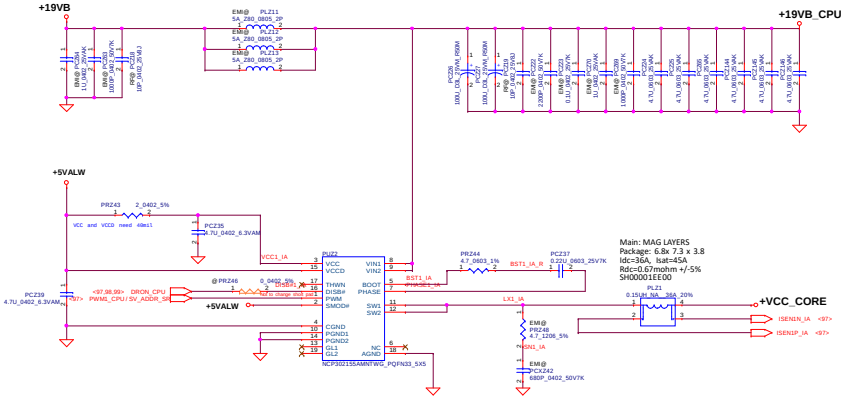
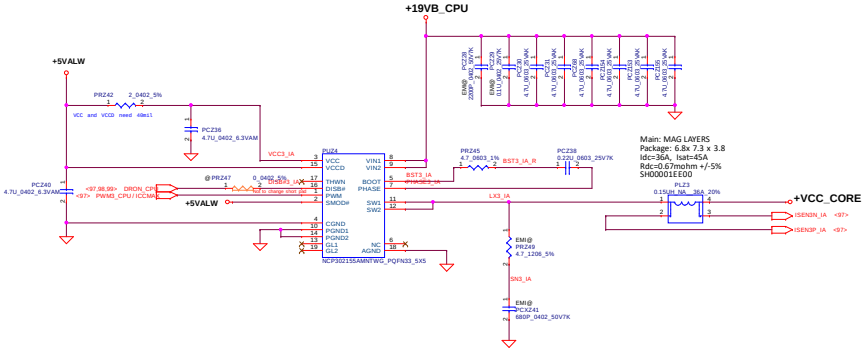
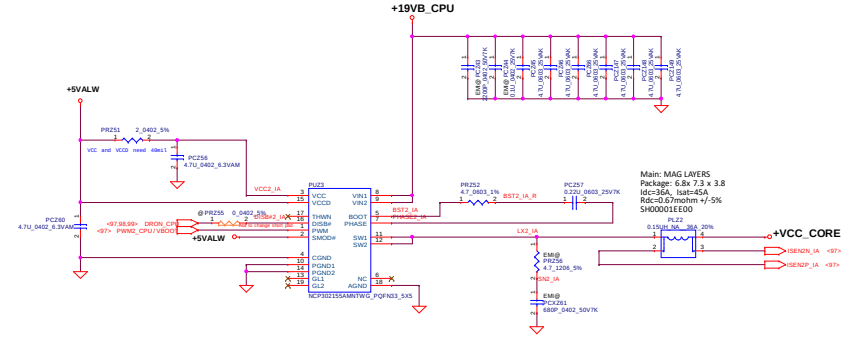
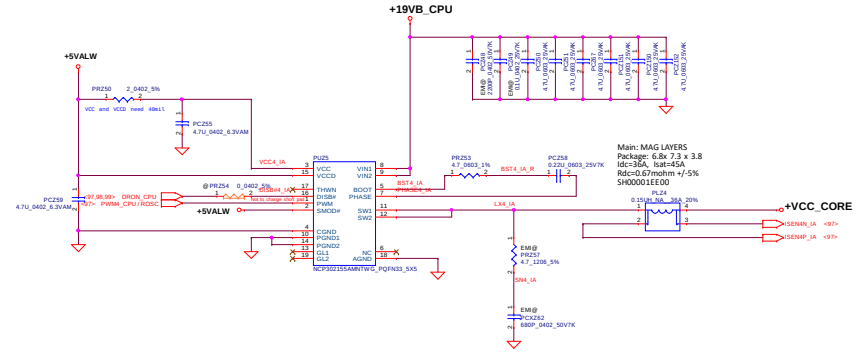
+VCCCORE
IPL2 = 93A
Peak Curren = 160A(ICCmax)
DC Load line: 2.1mohm
AC Load line: 2.1mohm
Current limit =208A(OCP)
FSW= 540 kHz









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Main Func = +VCCGT

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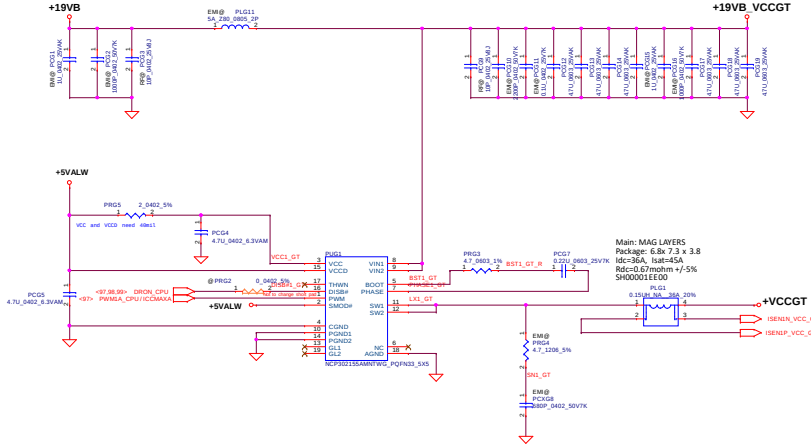
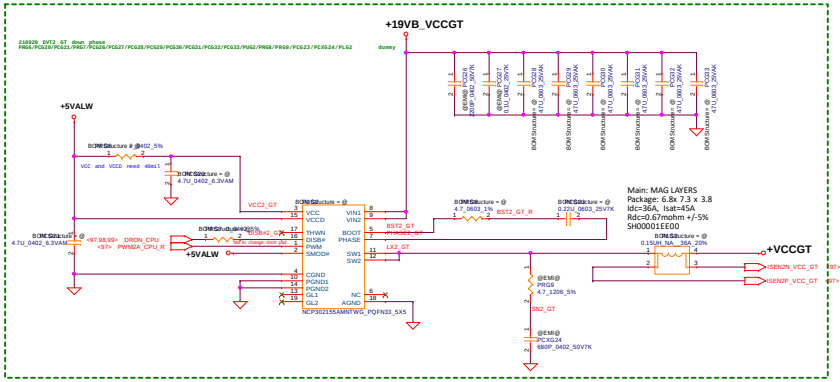
+VCCGT
IPL2 = 30A
Peak Curren = 50A(ICCmax)
DC Load line: 3.1mohm
AC Load line: 3.1ohm
Current limit =65A(OCP)
FSW= 540 kHz





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Main Func = +VCCIN DECOUPLING

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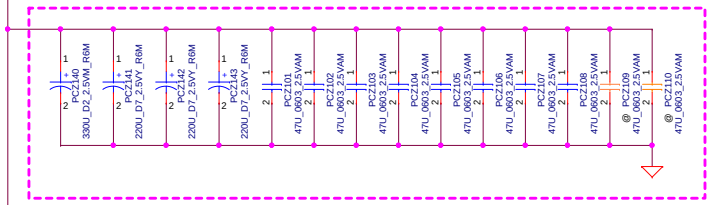
Intel ADL-P PDG Rev1.0 +VCC_CORE Output CAP :	Compal +VCC_CORE Output CAP :
CPU Primary Side: 330uF_D2 *3pcs 47uF_0603 *8 pcs	CPU Primary Side: 220uF_D7_2.5V_R6M *4pcs (1pcs reserved) 47uF_0603_2.5V_X6S *10pcs (2pcs reserved)
CPU Secondary side: 2.2uF_0402 *8pcs	CPU Secondary side: 2.2uF_0402_6.3V_X6S *8pcs

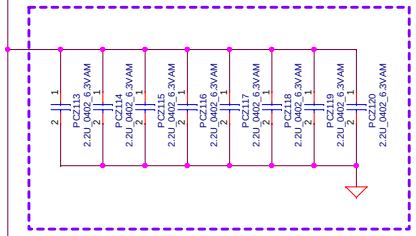
Intel ADL-P PDG Rev1.0 +VCC_GT Output CAP :	Compal +VCCGT Output CAP :
CPU Primary Side: 330uF_D2 *2pcs 47uF_0603 *8 pcs (1pcs reserved) 22uF_0402 *2 pcs	CPU primary side: 220uF_D7_2.5V_R6M *3pcs 47uF_0603_2.5V_X6S *8pcs (1pcs reserved) 22uF_0603_6.3V_X6S *2pcs
CPU Secondary side: 22uF_0402 *6pcs 10uF_0402 *4pcs (2pcs reserved)	CPU Secondary side: 22uF_0603_6.3V_X6S *6pcs 10uF_0402_6.3V_X6S *4pcs (2pcs reserved)

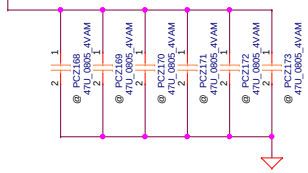
+VCC_CORE

CPU Primary Side



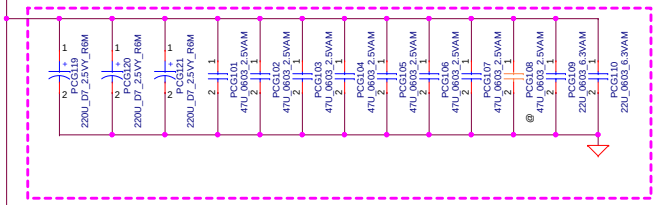
CPU Secondary side



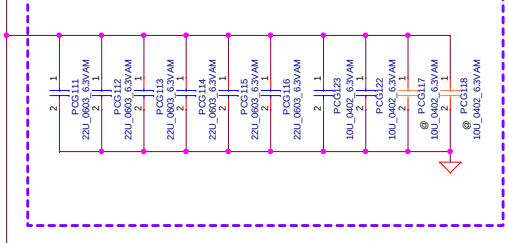


+VCCGT

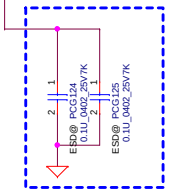
CPU Primary Side



CPU Secondary side



5/6 ESD Oliver requirement to add



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Title: PWR_CPU DECOUPLING

Size | Document Number: LA-L652P | Rev: 1.0(A00)

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Main Func = VGA CORE

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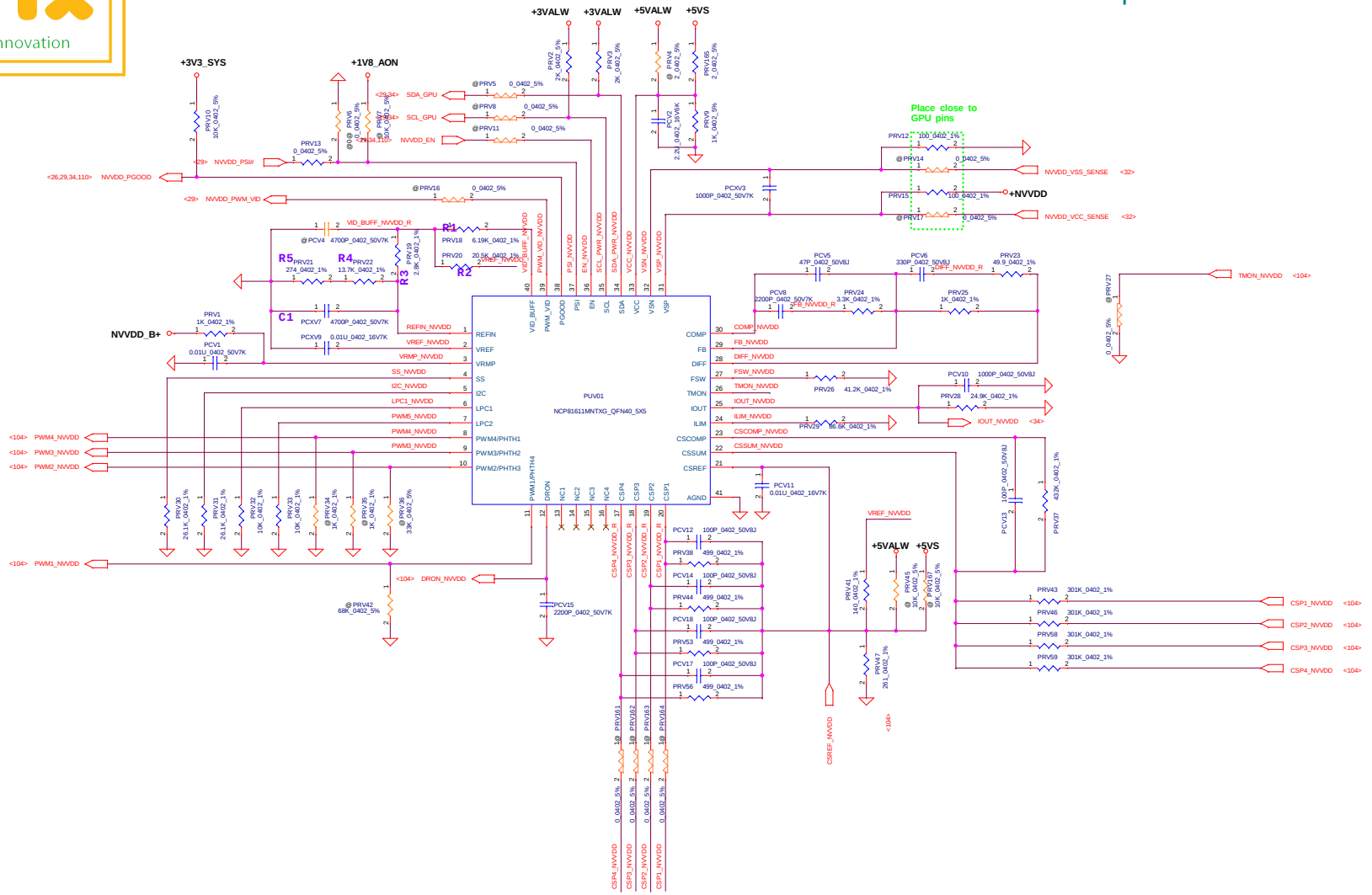
Config	
Vmin	0.3
Vmax	1.3
Vboot	0.75
R1	6.19K
R2	20.5K
R3	2.8K
R4	13.7K
R5	0.274K
C1	4.7n



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Compal Electronics, Inc.

Title: PWR_VGA_NCP81611MNTXG

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Main Func = GPU_CORE SW(1-4PH)

+19VB GPU_B+ NVDDD_B+ FBVDD_B+

Close to controller (PUV1) pin3

NVDD MOS

NVDD
TGP 80W
EDPc 75.1A
Peak Current 187.4A
OCP 244A
OCL 46.85A
Freq = 450 kHz

NVDD_B+

+5VS +5VALW

Use 0805 size

Main: MAG LAYERS
Package: 13.1 x 8.1 x 4
Idc=45A, Isat=77A
Rdc=0.48mohm +/-5%
SH00001QL00

+NVDDD

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Title: PWR_VGA_NCP30315

Size: LA-1652P | Rev: 1.0(100)

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Main Func = VGA CORE DECOUPLING

Nidvia ADL-P DG RevXX
+NVVDD Output CAP :

330uF_D2 *3pcs
47uF_0603 *8 pcs
2.2uF_0402 *8pcs

Compal
+NVVDD Output CAP :

330uF_D7_2V *4pcs
22uF_0805_6.3V_X6S *15pcs
10uF_0603_6.3V_X6S *34pcs
1uF_0402_6.3V_X6S *13pcs

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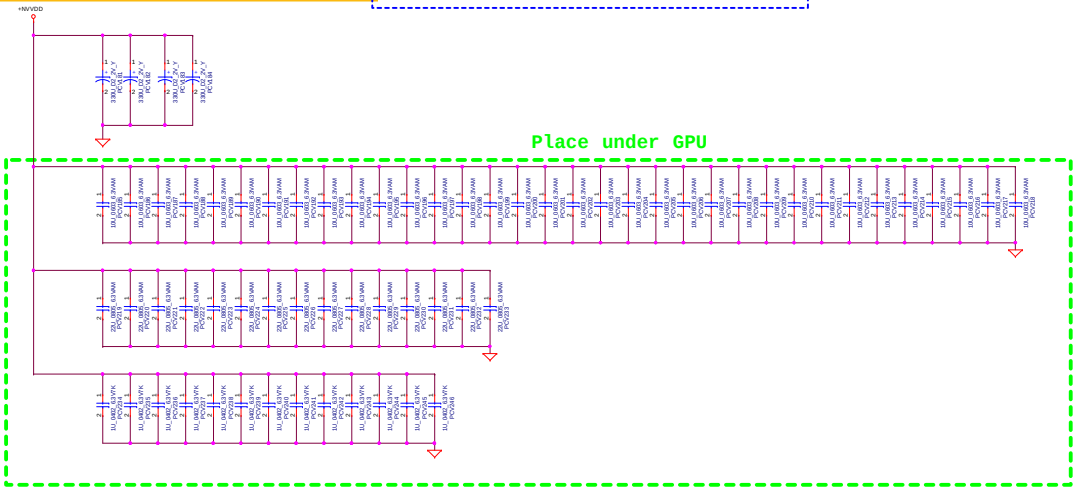

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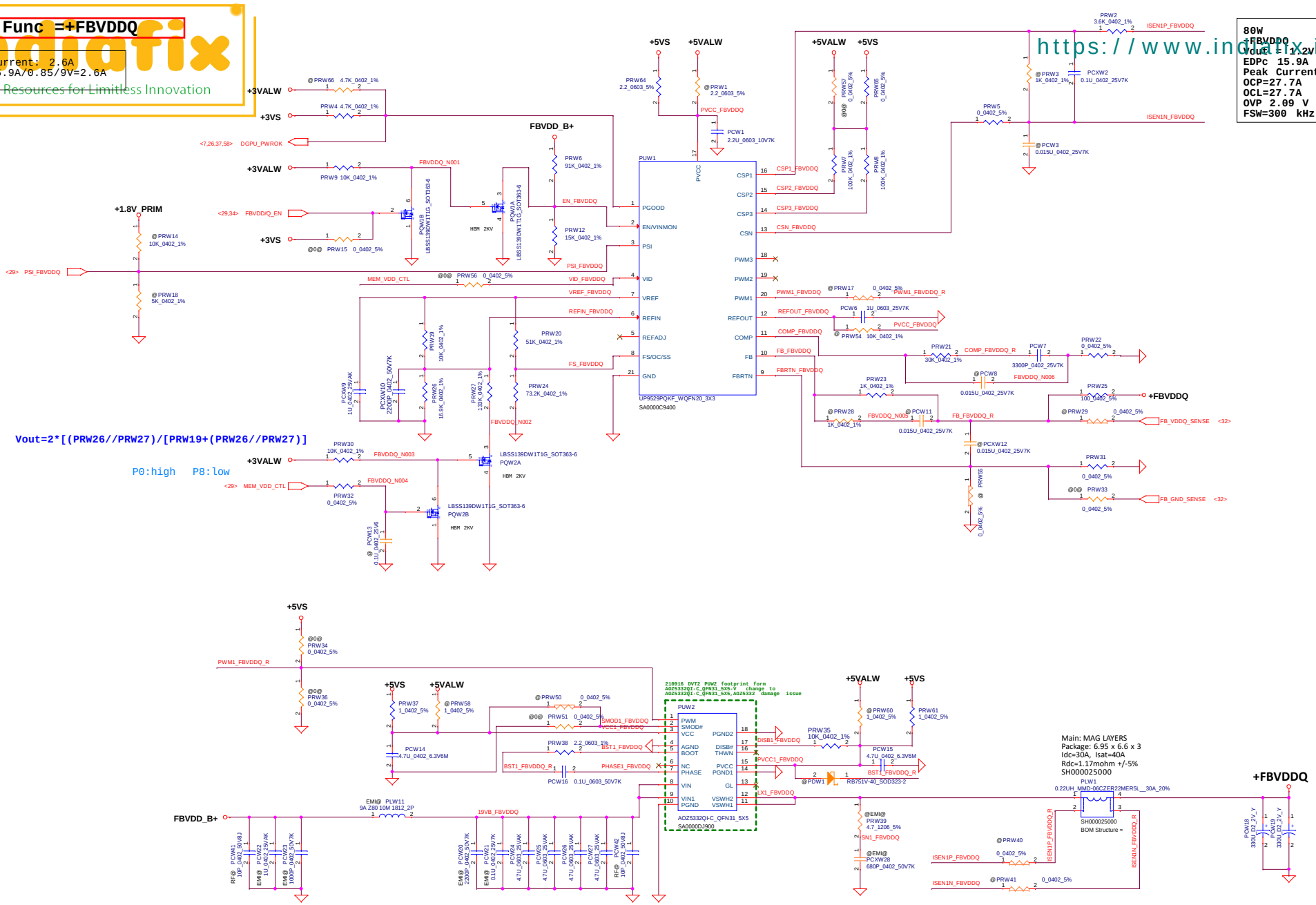
Main Func =+FBVDDQ

Input Current: 2.6A
1.25V*15.9A/0.85/9V=2.6A

80W
+FBVDDQ
Vout 1.2V ~ 1.25V
EDPc 15.9A
Peak Current 21.3A
OCP=27.7A
OCL=27.7A
OVP 2.09 V (155%)
FSW=300 kHz

Vout=2*[(PRW26//PRW27)/[PRW19+(PRW26//PRW27)]

P0:high P8:low



BOM config	GPU type	VRAM memory	VRAM vender	RVL	PRW19	PRW26//PRW27
	GN20P			1.25V	10K	16.9K
				1.2V	10K	16.9K//133K

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Title: PWR_+1.35VRAM

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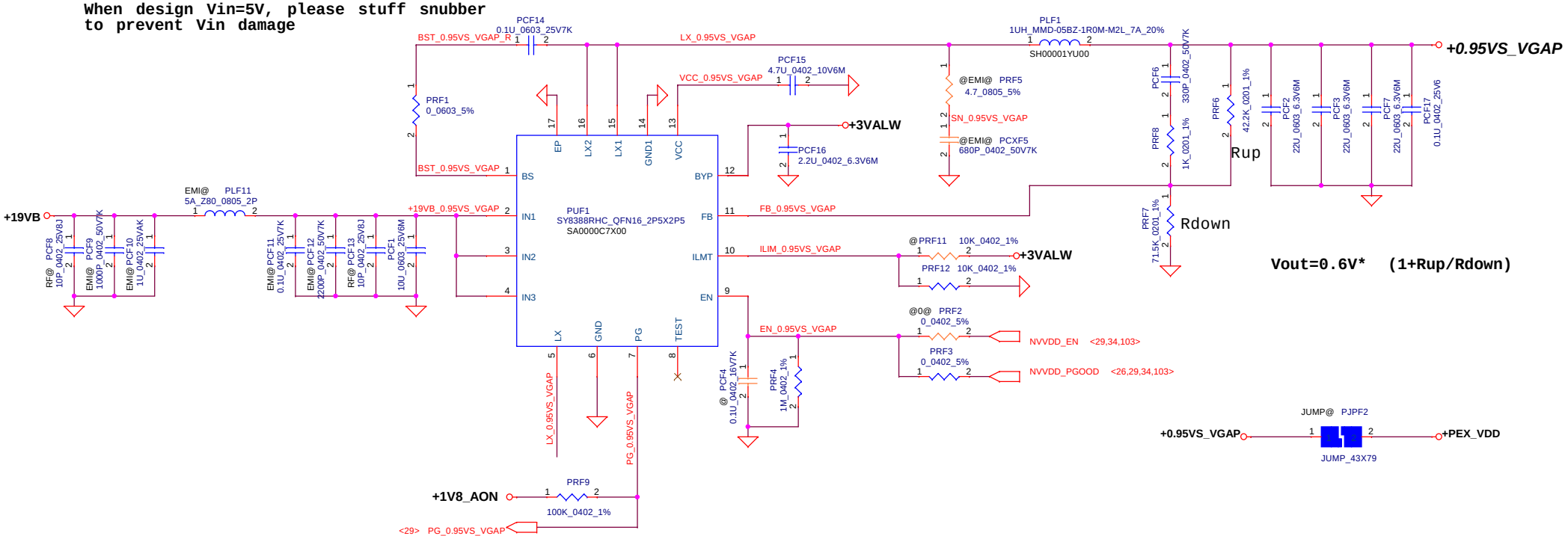
Main_Func =+0.95VS_VGAP

Input Current: 0.34A
0.95V*2.7A/0.85/9V=0.34A

+0.95VS_VGAP
TDC = 2.7A
Peak Current = 4.8A
OCP = 8A
Fsw=500 kHz

M1_CYNTEC_PCMB053T-1R0MS
M3_MAG_LAYERS_MMD-05CZ-1R0M-M7L
M4_CHILISIN_MHCI05030C-1R0M-R8
Package: 5.49 x 5.18 x 2
Idc=7A, Isat=13.7A
Rdc=18.9mohm +/-5%
SH00001YU00

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage



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Title: **PWR-+1.0VS_VGAP**

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Main Func = Smokeless UVP

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PU601 RT9069@smoke@ RT9069-33GB_SOT23_6P SA00008AU00

210706 DVT1 PU601 co-lay RT9069.
210713 DVT1 PU601 link SA0000ES010's footprint.
210719 DVT1 PR636, PR637 change to pop for setting AP2205's ADJ voltage.

210706 DVT1 change from SCS00000Z00 to SCS00005800_Vf value smaller.
210719 DVT1 PD613 change to pop.
210720 DVT1 PD612 change to un-pop.

+12.6V_BATT
+5VALW
+19V_VIN
+3.3V_PWRSRC_LDO
+3VLP
+3VALW
+3.3V_PWRSRC_IN
+3.3V_PWRSRC_EC

Need to short

AZV3002
Icc=12uA_max
Vout=3.15V@Vcc=3.3V and Io=3mA

+VCC_CORE OVP
Vref = Min. , Typ. , Max.
VIN = Min., Typ. , Max.

+NVVDD OVP
Vref = Min. , Typ. , Max.
VIN = Min. , Typ. , Max.

RB520SM
Vf =0.29V@1mA
Ir =1uA @Vr=10V

AC_UVP_Protect

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Title: **PWR- Smokeless UVP/OVP**

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